NASA CR - 145008

FINAL REPORT

PHASE I

Optimization of Solar Cells for Air Mass Zero Operation and a Study of Solar Cells at High Temperatures.

NASA Contract NASI-12812

Principal Investigators - H. Hovel, J. M. Woodall

Work Performed by

Exploratory Materials and Devices Project

IBM Research Laboratory

Yorktown Heights, New York.

National Aeronautics and Space Administration

THE OPTIMIZATION OF $Ga_{1-x}Al_xAs$-GaAs SOLAR CELLS FOR AIR MASS ZERO OPERATION AND A STUDY OF $Ga_{1-x}Al_xAs$-GaAs SOLAR CELLS AT HIGH TEMPERATURES

By H. J. Hovel and J. M. Woodall

IBM Thomas J. Watson Research Center

Yorktown Heights, New York 10598

Background and General Objectives

High efficiency solar cells based on a material such as GaAs have been sought for many years but have proved to be elusive in the past. GaAs has several advantages over Si for use as a solar cell; these include higher maximum efficiency, improved performance at high temperatures, higher output voltage, superior resistance to degradation from particle radiation, and a potentially better power to weight ratio. However, there are several major problems associated with GaAs which have prevented the realization of these advantages. The first problem is surface recombination. GaAs has much shorter lifetimes and higher surface recombination velocities than Si, while at the same time the optical absorption is high. Most of the charge carriers in GaAs solar cells are generated within 2 microns of the surface, and surface recombination losses therefore have a strong effect on the collection efficiency. (By contrast, significant numbers of carriers are generated over 100 to 200 micron distances in Si, and surface processes have a smaller effect.) In order to minimize the surface recombination problem

in GaAs, the junction depth (depth of the junction depletion region beneath the surface) must be made small; however, this introduces the second major problem, that of series resistance. If the sheet resistance of the surface region is high, the resulting high series resistance will reduce the available output power. This can only be partly compensated by higher doping levels, since higher doping levels mean shorter minority carrier diffusion lengths and reduced collection efficiency. A compromise must be made between large junction depths and high doping levels to minimize series resistance and small junction depths and low doping levels to maximize collection efficiency. The end result is that the power conversion efficiencies of GaAs solar cells have been less than those of Si cells, and most of the work in solar cells in the past 10 years has therefore been concentrated on Si.

It has been recently demonstrated that the two major problems limiting GaAs cells can be minimized by the use of a thin, transparent layer of p-type $Ga_{1-x}Al_xAs$ on the surface of the GaAs p-n junction. The lattice of the alloy layer matches that of the GaAs very closely, which greatly reduces the recombination velocity at the interface between the two materials (which is now the "surface" of the GaAs p-n junction) and therefore reduces the surface losses. In addition, the p-type $Ga_{1-x}Al_xAs$ forms an ohmic contact to the p-type GaAs surface region, and since the sheet resistivity of this alloy layer can be made low, the series resistance in the device is considerably reduced for a given doping level in the GaAs. The $Ga_{1-x}Al_xAs$ is transparent to photons with energies below 2.1 eV and the absorption increases slowly with increasing energy above 2.1 eV. The result is that

solar cells consisting of $pGa_{1-x}Al_xAs$-pGaAs-nGaAs have exhibited efficiencies of over 16% in sunlight at Air Mass 1 and 20% at Air Mass 2 or higher at room temperature[1,2,3] and almost 6% at Air Mass 1 at 300°C.[4]

This new type of solar cell outlined above exhibits considerably higher efficiencies when measured in sunlight within the earth's atmosphere than any previous solar cells of Si or GaAs. It is the purpose of this contract to develope the techniques and procedures which are expected to result in the optimization of this new type of solar cell for operation at Air Mass 0 (outer space environment). It is also the purpose of this contract to develope fabrication techniques which should allow the devices to operate continuously at high temperatures (T = 300°C or higher). Three types of structures are to be investigated: one consisting of a nGaAs substrate, a Zn doped pGaAs region, and a Zn doped $Ga_{1-x}Al_xAs$ layer, the second consisting of an nGaAs substrate, a Ge doped pGaAs region, and a $pGa_{1-x}Al_xAs$ upper layer, the third consisting of an n^+GaAs substrate, an $nGa_{1-x}Al_xAs$ region, a $pGa_{1-x}Al_xAs$ region, and a $pGa_{1-y}Al_yAs$ upper layer. In all three cases, the upper alloy layer is thin and of high Al composition in order to obtain high spectral response over the widest possible range of photon energies. Spectral response, capacitance-voltage, current-voltage, diffusion length, sunlight (or the equivalent)-efficiency, and efficiency-temperature measurements will be made as a function of device parameters in order to analyze and optimize the solar cell behavior.

Liquid Phase Epitaxial Growth Experiments

At present, the most successful technique for growing $Ga_{1-x}Al_xAs$ layers on GaAs is liquid phase epitaxy (LPE). This is a solution growth method in

which $Ga_{1-x}Al_xAs$ deposits from Ga rich melts onto a GaAs substrate as a result of slowly cooling the melt from an initial high temperature. A considerable amount of effort was devoted towards developing this method to produce uniform $Ga_{1-x}Al_xAs$ layers, $0.75 < x < 1$, as free as possible from metallurgical defects, and with a $Ga_{1-x}Al_xAs$ layer thickness control of $0.5\mu \pm 0.1\mu$.

Fixture Description

Three different apparatus were evaluated during the contract period and are shown schematically in Fig. 1. The fixture in Fig 1a was fabricated from high purity, high density Poco graphite. The GaAs substrate is mounted on the face of a rotable inner cylinder, while the outer cylinder with six melt chambers is held fixed. Each melt chamber contains a slot whch holds a slab of GaAs, the As source for the Ga, Al, As melts. The substrate holder contains a thin walled "moat" which is filled with Ga in order to uniformly heat sink the GaAs substrate and thus prevent undesirable temperature gradients. Rotation of the substrate holder was accomplished via a high purity molydenum fixture, a rod portion 1/4" diameter x 24" in length and a portion which fits into the graphite substrate holder. (There was no evidence that the molydenum part contributed any undesirable impurities to the solar cells grown in this fixture.) The growth fixture is contained by a fused quartz tube which is purged with either hydrogen or 90% nitrogen, 10% hydrogen high purity gas.

The second fixture used for this study is shown in Fig. 2b. This fixture contains only three melt chambers. The substrate holder is also rotatable. However, in this case the GaAs substrate lies in the horizontal

plane. This fixture is composed of both Poco graphite and pyrolytic boron nitride parts in such a way that both the GaAs substrate and the melts are only in contact with BN surfaces. A majority of the LPE experiments in this study were performed using this fixture. The reasons for this are described later. As in the case for the fixture in Fig. 1a, rotation was effected using a 1/4" moly rod. The last LPE fixture used is shown in Fig. 1c. It is similar to the one in Fig. 1b except that it contains six melt chambers, has no BN parts, and the substrate is heat sinked by a moly substrate holder separated by a 0.010" graphite plate to prevent direct contact between the GaAs substrate and the moly substrate holder. Further reference to these fixtures in Fig. 1 will be denoted as follows: Fig. 1a - "crucible 1", Fig. 1b - "crucible 2" and Fig. 1c -"crucible 3".

Substrate Preparation

Since the GaAs substrate is an important part of the p-$Ga_{1-x}Al_xAs$, p-GaAs, n-GaAs cell structure formed by a one step liquid phase epitaxy growth procedure, it is important that the substrate be prepared in a manner that will render the surface free from mechanical damage, dirt, excessive oxidation, non-uniform roughness, and chemical contamination which can cause a deterioration of minority carrier diffusion lengths in the substrate during growth of the epitaxial layer. Surface contamination and imperfections can lead to non-uniform growth. The substrate preparation procedure found to be the most effective is shown in Table 1. The purpose of the organic solvent cleaning steps is to remove dirt, grease and stains from the surface prior to the final preparation of the surface. It is important that the transfer from one solvent to the next be done in a manner which prevents the

solvent from evaporating away from the surface of the substrate. Evaporation of the solvent leaves a residue on the wafer which may not be dissolved by the next solvent. This is easily prevented by pouring off all but a small amount of solvent covering the substrate and then quickly rinsing it with the next solvent to be used. After Step F the wafer is clean except for uncontrolled oxidation. The purpose of the remaining steps is to remove these oxides and replace them with a controlled oxide layer which is then chemically removed prior to loading into the fixture. There are two different procedures which can be used depending on how much etching of the surface can be tolerated. When etching is allowable, Steps G through K are used. These steps remove uncontrolled oxides and polish-etch away a few microns of surface leaving it nearly oxide free. When no etching is desired, Step L is initiated directly after Step F. The purpose of Steps L-R is to cover the surface of the clean substrate with a 900-1000Å oxide which is then removed immediately before loading into the growth apparatus. After Step N, it is possible to store the anodized substrate until it is needed. After Step Q, the blowing dry of the substrate, it is important to minimize the exposure of the substrate to a dirty air environment. For nearly all the experiments, GaAs (100) n-type substrates 0.3" x 0.5" x 0.020" in dimension were used.

Fixture Preparation

All of the fixtures used in this study have component parts which are fabricated of high purity, high density graphite. This graphite is somewhat porous and will easily absorb water vapor and air during leading. This absorbed water and oxygen is released during the heat up phase of the growth

cycle. This water and oxygen can cause oxide formation on the substrate and melt surface. This may not be a severe problem with respect to the substrate since the high purity H_2 or H_2 - N_2 mixtures are flowing through the apparatus during growth will reduce the oxides on the substrates. However, the oxides which form on the LPE melts contain Al and are not easily reduced by H_2. It was found in this study that excessive oxidation of the Ga-Al-As LPE melts was the single most important factor contributing to non-uniform epitaxial growth of $Ga_{1-x}Al_xAs$ layers.

Since the Al in the LPE melts is a very effective "getter" of oxygen, it is also necessary to minimize oxygen from sources other than the graphite. The other main sources are: 1) oxygen and water in the gases, 2) oxides on the Ga, and 3) oxygen from the SiO_2 apparatus. This first source is minimized by passing gas with $\leq$ 1 ppm oxygen and water vapor through a liquid N_2 trap and an oxysorb trap, a reactive molecular sieve material, prior to flowing it through the LPE apparatus. The second source can be controlled by baking the Ga above 800°C in either vacuum or H_2 gas. The last source can be controlled by maintaining the SiO_2 apparatus below 900°C when purging with H_2 gas. If higher temperatures are required, purging with inert gases is necessary to prevent excessive oxidation (i.e. generate oxygen sources which react with the melt).

In this study two different procedures were adopted to control melt oxidation:

1. Overnight bake out of fixture containing Ga LPE melt component at 900°C in vacuum or H_2 gas. Purge at room temperature with H_2 then solidify Ga. Load apparatus with remaining components.

2. Overnight bakeout of fixture in vacuum at 900°C. Back fill with H_2 gas. Load apparatus with growth components, with Ga component seperate from other components. Purge with H_2 and heat to 800°C for 1 hr so that oxides on Ga will be removed. Continue with LPE growth schedule.

Common to both these procedures is the removal of major oxygen sources prior to contact with the Al component in the melt. The importance of this point cannot be over emphasized.

Melt Preparation

The preparation of the LPE melts is determined by four factors: the fixture used, the growth temperature, the composition of the $Ga_{1-x}Al_xAs$ and x_j, the thickness of the Zn diffused p-GaAs layer. Selection of the growth temperature is influenced mainly by the value of previous results, control of the $Ga_{1-x}Al_xAs$ layer thickness, growth morphology and x_j control. Most of the experiments in this study were performed at growth temperatures at or near 900°C. Once the $Ga_{1-x}Al_xAs$ composition has been selected, the Ga-Al-As concentrations needed for the melt are determined by reference to the data in Table 2. The first column of this table shows the weight (in grams) of Al needed per gram of Ga to form a melt which when saturated with GaAs at 900°C will grow a $Ga_{1x-}Al_xAs$ layer of the desired composition, (Column 2). The data for this is taken from reference 7. Column 3 shows the thickness in microns of the $Ga_{1-x}Al_xAs$ grown layer per gram of Ga, per °C of cooling, per cm^2 of substrate area. A typical melt would contain the following components:

Ga - 1.9 gms
Al - 0.027 gms
Zn - 0.027 gms
GaAs - excess amount (source bar)

A 0.5°C cool of this melt when saturated at 900°C in contact with a 0.2" x 0.5" GaAs (100) substrate would result in a $Ga_{1-x}Al_xAs$" layer with $x \approx 0.85$ and a thickness of $\sim 0.5\mu$. Also, x_j would be about 3μ depending on the melt saturation and growth programs.

LPE Growth Schedule

A flow diagram for the LPE growth of a $pGa_{1-x}Al_xAs$-pGaAs-nGaAs solar cell structure is shown in Table 3. It is desirable to minimize exposure of the fixture, melt components, and substrates to a dirty air invironment. Thus, if possible, the loading of the fixture and assembling of the apparatus should be done on a dust free bench, purged with inert gas or dust free air.

The main part of the LPE growth schedule is the time-temperature program and fixture operation which produces the layer growth. In this study, four basic procedures which were studied and are shown schematically in Fig. 2-5 The schedule in Fig. 2 was used early in the investigation for about 19 LPE runs. This schedule can be discussed in five parts. Part one is the evacuation of the apparatus to about 5μ of Hg pressure and backfill with H_2 gas. This is done twice and its purpose is to rid the fixture and apparatus of as much water and oxygen as possible prior to heat up. Part two is the insertion of the apparatus into the furnace and bringing it to the desired saturation temperature. In part three the GaAs source bar saturates the melts. This happens by one of two mechamisms: 1) a source bar already placed in the melt chamber or 2) by rotating a source bar in the substrate holder into the melt position. Indexing is accomplished by aligning a barrel angle indicator fixed to the rod which rotates the substrate

holder with a fiduciary mark on a fixed lens. Generally, due to the symmetry of the three crucibles used in this study, position changes require rotations of some multiple of 30°.

Part 4 brings the substrate into contact with the melt. During parts 3 and 4 the temperature of the apparatus is maintained constant with ±0.1°C. The main purpose of part 4 is to "getter" or "leach" away possible undesirable impurities from the surface of the substrate which could have contaminated during parts 2 and 3, or could have been in the substrate originally. Part 5 is the cooling step which causes the $Ga_{1-x}Al_xAs$ layer to form. After step 5 the wafer is rotated away from the melt chamber prior to removing the apparatus to room temperature. Any melt in contact with the substrate during this cooling step causes unwanted growth.

The schedule in Fig. 2 was later abandoned in favor of one which gave better control over the melt saturation step.

The schedule in Fig. 3 is the one used for the so called "leaching" experiments described in a later section. It is the same as Fig. 2 except that there is no cooling step to cause a $Ga_{1-x}Al_xAs$ layer to grow.

The schedule in Fig. 4 is the one which was used the most in this study. It produced the most reproducible layer thickness, surface morphology and x_j. Part 1 is the same as for the previous schedules. Part 2 is the 1 hour 800°C Ga bake step in which oxides are removed prior to bringing the Al and GaAs source bar into the melt. Part 2 is used only in conjunction with LPE runs in H_2 which has a cavity in the substrate holder for containing the Al separately from the melt. For crucibles 1 and 3, the Al is

added to a Ga melt which has been previously baked out over night during the loading step. In part 3 the Al then the GaAs sources are brought in contact with the melt and held at constant temperature (usually 915°C) for 30 minutes to effect saturation. Next the melt is cooled at 0.5°C/min. for 30 minutes with the GaAs source bar still under the melt to effect finer saturation control (part 4). In step 5 the substrate is brought into contact with the melt at constant temperature (usually 900°C) and held there for between 10 and 60 minutes. Next in step 6 the melt is cooled ∿0.5°C at 0.1°C/min. The substrate is then moved away from the melt and the apparatus removed from the furnace.

The schedule in Fig. 5 is the same as Fig. 4 except that in step 5 when the substrate is brought into contact with the melt, the temperature of the melt is increased instead of remaining constant. This produces an etch back of substrate prior to layer growth and, based on previous results may have a beneficial effect on device performance.

Table 4 lists the crystal growth and metallurgical characterization summary of the LPE runs made during this investigation. Runs SCB1-19 were aimed primarily at establishing the effects of crucible preparation procedures, and LPE growth program on the performance of the $pGa_{1-x}Al_xAs$, p-GaAs, nGaAs solar cell structure. Runs SCB20-36 were performed to determine the effects of "leaching" on the hole diffusion lengths in n-type substrates with poor starting diffusion lengths. Runs SCB37-77 were aimed at fabricating the target cell structures for this contract.

Table 5 lists the qualitative and quantitative device characteristics of the runs which were fabricated into devices and studied. Details of these runs are discussed below.

Leaching Experiments

During the course of this investigation it was determined that the substrates which were being used for the Zn diffused pGaAlAs-pGaAs-nGaAs structure had hole diffusion lengths of less than one micron. Such small diffusions precluded fabrication of high efficiency AMO cells. Until better substrates became available it was decided to test the validity of a useful working hypothesis: holding a substrate of GaAs with poor hole diffusion lengths in contact with a Ga-Al-As melt with a composition to give $Ga_{1-x}Al_xAs$ solid composition of $0.75 \leq x < 1$ might "leach out" detrimental impurities from the substrate near the surface or perhaps might result in an improvement of the diffusion length near the surface. The experiments were performed using the schedule in Fig. 3. The melts were based on 1.5 gms Ga and 0.022 gms Al. The leaching temperature was 900°C and the times were 0, 2.5 and 12.7 hours. The results are shown in Table 6 which also compares the leaching results with several control samples. The diffusion length measurements were made by A. Sekela of Carnegie-Mellon University using an electron beam probe technique. It is seen that the results are somewhat inconclusive. The sample p-Si-97 with a low starting value shows considerable improvement whereas sample 424L with a higher starting value shows no significant change. A tentative conclusion is that the results are initial value dependent, and that leaching might produce better diffusion lengths for leaching times much longer than 12.7 hours at 900°C.

Theoretical Aspects of the Solar Cell Collection Process.

The p$Ga_{1-x}Al_xAs$-pGaAs-nGaAs solar cell has been analyzed theoretically in a paper given by Hovel and Woodall at the 10th IEEE Photovoltaics Specialists Conference in Palo Alto.[1] The spectral responses, short circuit currents, and efficiencies were computed for the simplest form of these devices in which the three regions are each uniform in composition, doping, mobility, and lifetime. The recombination of carriers at the $Ga_{1-x}Al_xAs$ surface and at the $Ga_{1-x}Al_xAs$-GaAs interface and the collection of some of the photogenerated carriers from the $Ga_{1-x}Al_xAs$ were included in the model.

The energy band diagram of a $Ga_{1-x}Al_xAs$-GaAs solar cell in equilibrium is shown in Figure 6. When electron-hole pairs are generated in the GaAs, holes diffuse from the n region into the pGaAs region while electrons from the pGaAs diffuse into the nGaAs region. Photogenerated electrons in the conduction band of the pGaAs region are prevented from entering the $Ga_{1-x}Al_xAs$ layer by the energy barrier ΔE_c at the interface, and the only potentially significant loss of carriers at this interface is therefore due to interface recombination. Electron tunneling through the $Ga_{1x-}Al_xAs$ to the upper surface should be negligible for $Ga_{1x-}Al_xAs$ thicknesses greater than 100 Å, and multistep tunneling (present in many heterojuctions) should be negligible due to the high perfection of the structure and the resulting lack of defect states.[2]

Free electrons photogenerated in the $Ga_{1-x}Al_xAs$ layer can diffuse to the interface and enter the pGaAs region, contributing to the photocurrent. Recombination in the bulk and at the upper surface represent the major losses of these carriers. The sudden drop in potential energy makes the interface an effective "sink" for electrons analogous to the depletion region edge on

the p-side of the junction. The excess electron density in the $Ga_{1-x}Al_xAs$ can be assumed to be reduced to a negligible value at the interface, therefore.

Collection from the $Ga_{1-x}Al_xAs$.

The continuity equation for the excess photogenerated electrons is:

$$D_a \frac{d^2\Delta n}{dx^2} + \beta F(1-R)\, e^{-\beta x} - \frac{\Delta n}{T_a} = 0 \qquad (1)$$

where F is the incident photon flux, R is the reflection coefficient, β is the absorption coefficient in the $Ga_{1-x}Al_xAs$, D_a is the electron diffusion coefficient, and T_a is the electron lifetime. The origin, x = 0, is taken at the surface. No electric field or composition gradient has been assumed.

The boundary conditions are:

$$S_a \Delta n = D_a \frac{d\Delta n}{dx} \qquad [x = 0] \qquad (2)$$

$$\Delta n = 0 \qquad [x = D^-] \quad . \qquad (3)$$

Solving (1) with (2) and (3) yields the photocurrent from the $Ga_{1-x}Al_xAs$:

$$J_{D^-} = \frac{qF(1-R)\beta L_a}{(\beta^2 L_a^2 - 1)} \left[\frac{\beta L_a + S_a \frac{T_a}{L_a}(1 - e^{-\beta D}\cosh\frac{D}{L_a}) - e^{-\beta D}\sinh\frac{D}{L_a}}{S_a \frac{T_a}{L_a}\sinh\frac{D}{L_a} + \cosh\frac{D}{L_a}} - \beta L_a\, e^{-\beta D} \right] \qquad (4)$$

where L_a is the diffusion length, $L_a = \sqrt{D_a T_a}$. This flow of electrons is injected into the pGaAs at the interface.

Collection from the GaAs.

In the pGaAs, the minority carrier continuity equation is:

$$D_g \frac{d^2\Delta n}{dx^2} + \alpha F(1-R)\, e^{-\beta D}\, e^{-\alpha(x-D)} - \frac{\Delta n}{T_g} = 0 \qquad (5)$$

where D_g and T_g are the diffusion coefficient and lifetime in the pGaAs. The reflection of light at the interface (x=D) has been neglected due to the closeness of the refractive indices. The boundary conditions are

$$D_g \frac{d\Delta n}{dx} = S_g \Delta n - \frac{J_D^-}{q} \qquad [x = D^+] \qquad (6)$$

$$\Delta n = 0 \qquad [x = D + x_j] \qquad (7)$$

where S_g is the interface recombination velocity, and x_j is the junction depth below the interface. Solving (5), the photocurrent at the junction edge is:

$$J_{D+x_j} = \frac{qF(1-R)\, e^{-\beta D}\, \alpha L_g}{(\alpha^2 L_g^{\,2} - 1)} \left[\frac{\alpha L_g + S_g \frac{T_g}{L_g}\left(1 - e^{-\alpha x_j} \cosh \frac{x_j}{L_g}\right) - e^{-\alpha x_j} \sinh \frac{x_j}{L_g}}{S_g \frac{T_g}{L_g} \sinh \frac{x_j}{L_g} + \cosh \frac{x_j}{L_g}} - \alpha L_g\, e^{-\alpha x_j} \right] + \frac{J_D^-}{S_g \frac{T_g}{L_g} \sinh \frac{x_j}{L_g} + \cosh \frac{x_j}{L_g}} \; . \qquad (8)$$

The second term in (8) describes how the extra carriers injected from the $Ga_{1-x}Al_xAs$ are attenuated by the interface and bulk recombination before they can reach the junction edge.

The photocurrent collected from the base (nGaAs) is calculated using analagous continuity equations and boundary conditions:

$$D_p \frac{d^2\Delta p}{dx^2} + \alpha F(1-R)\, e^{-\beta D}\, e^{-\alpha x_j}\, e^{-\alpha W}\, e^{-\alpha x} - \frac{\Delta p}{T_p} = 0 \qquad (9)$$

where W is the depletion width, and the origin has been moved to the depletion region edge on the n-side for convenience.

The boundary conditions are

$$\Delta p = 0 \qquad [x = 0] \qquad (10)$$

$$S_p \Delta p = -D_p \frac{d\Delta p}{dx} \qquad [x = H'] \qquad (11)$$

where S_p is the recombination velocity at the back surface and H' is the width of the base except for the depletion region, $H' = H - (D + x_j + W)$, where H is the total device thickness. The photocurrent from the base is then

$$J_p = \frac{qF(1-R)\, e^{-\beta D}\, e^{-\alpha x_j}\, e^{-\alpha W}\, \alpha L_p}{(\alpha^2 L_p^2 - 1)} \left[\alpha L_p - \frac{\frac{S_p L_p}{D_p}\left(\cosh\frac{H'}{L_p} - e^{-\alpha H'}\right) + \sinh\frac{H'}{L_p} + \alpha L_p\, e^{-\alpha H'}}{\frac{S_p L_p}{D_p}\sinh\frac{H'}{L_p} + \cosh\frac{H'}{L_p}} \right] \qquad (12)$$

which reduces to

$$J_p = \frac{qF(1-R)\ e^{-\beta D}\ \alpha L_p}{(\alpha L_p + 1)}\ e^{-\alpha(x_j + W)} \tag{13}$$

when the thickness H' is much larger than a diffusion length.

The current from the depletion region is:

$$J_W = qF\ e^{-\beta D}\ e^{-\alpha x_j}\ (1-e^{-\alpha W})\ (1-R) \tag{14}$$

and the overall photocurrent is the sum of the photocurrents evaluated at the junction edge:

$$J_{ph}(\lambda) = J_{D+x_j}(\lambda) + J_W(\lambda) + J_p(\lambda) \tag{15}$$

where the usual assumption has been made that the photocurrents J_p and J_{D+x_j} are constant across the depletion region, i.e. no recombination of the photogenerated electrons takes place within the depletion region.

Spectral Response

The analysis above was used to evaluate the expected behavior of $Ga_{1-x}Al_xAs$-GaAs solar cells for various junction depths, $Ga_{1-x}Al_xAs$ layer thicknesses, and GaAs material properties. An example of the results was presented at the 10th IEEE Photovoltaics Conference.[1] The absorption coefficients[1] of GaAs and $Ga_{1-x}Al_xAs$ are given in Figure 7. Figure 8 illustrates the spectral response (carriers collected/photon) for various $Ga_{1-x}Al_xAs$

thicknesses for devices with the properties given in Table 7. The $Ga_{1-x}Al_xAs$ bandgap causes the response to cut-off at 2.4-2.5 eV for thick alloy layers; this cut-off moves to higher energies as the layer thickness is decreased. Most of the cut-off is due to the direct bandgap of the $Ga_{1-x}Al_xAs$ (2.7 eV), since this is the most strongly absorbing energy band. As the $Ga_{1-x}Al_xAs$ thickness is reduced below 1 micron, the direct bandgap absorption becomes less important (since it increases slowly with energy above 10^4 cm^{-1}) and the spectral response increases rapidly with decreasing thickness. Most of this increased response is due to greater penetration of light to the underlying GaAs p-n junction, although some of it can be attributed to increased collection of carriers generated in the $Ga_{1-x}Al_xAs$.[1]

The measured spectral responses of three $Ga_{1-x}Al_xAs$-GaAs solar cells are shown in Figure 9 for devices with (approximately) the same junction depth but with varying $Ga_{1-x}Al_xAs$ thicknesses. The increase in high energy response for thinner alloy layers is clearly seen. Evidence of the high energy "saturation" of the response (predicted in Figure 8) for layers less than 1μ thick is also seen.

The spectral responses of cells with narrow and deep junctions are shown in Figure 10. These cells were made on substrates with poor diffusion lengths (0.4-0.6μ), and under these circumstances the best responses are obtained by minimizing the number of carriers generated in the nGaAs region. Cells with junction depths less than 0.5μ made on these substrates behaved very poorly, exhibiting a slowly rising response with increasing energy and a low peak magnitude (peak absolute quantum efficiency 0.4-0.5). This is expected[3] from the poor collection at long wavelengths where carriers are

generated from 1-2 microns from the interface. Deep junctions (2.5μ to 3.5μ) lead to much better long wavelength collection but a gradually decreasing response at higher energies where most carriers are generated near the interface and far from the junction edge. Device SCB62 in Figure 10 is typical of deep junction cells and typical of most of the devices obtained during the contract period. The best overall response on poor quality substrates is obtained if the junction depth lies in the intermediate range of 1.0-1.3μ (SCB46 in Figure 10). High quality substrates lead to slightly better long wavelength response and higher peak quantum efficiencies (0.9 instead of 0.8); nevertheless it is valuable to note that good devices can be made on poor substrates by the combination of thin $Ga_{1-x}Al_xAs$ layers and intermediate junction depths. Further discussions of devices made on poor quality substrates are given in the Appendix.

Photocurrent

The theoretical short circuit photocurrent under any combination of $Ga_{1-x}Al_xAs$ thickness, junction depth, and device diffusion lengths can be found by integrating the spectral response, $J_{ph}(\lambda)/qF(\lambda)$, over the AM0 spectrum:

$$J_{ph}(AM0) = q\int_0^\infty [J_{ph}(\lambda)/qF(\lambda)]\cdot F_\lambda(AM0)\cdot d\lambda \qquad (16)$$

where $J_{ph}(\lambda)$ is given in equation (12). The solar spectrum for AM0 conditions was taken from Thekaekara.[4] The computed short circuit currents as a function of junction depth and alloy layer thickness for the conditions of Table 1 are shown in Figure 11. The current peaks at a junction depth of

around 0.4 microns for the relatively good base diffusion length (2μ) assumed in the calculations; as the ratio of base region diffusion length to top region (pGaAs) diffusion length becomes smaller, the peak shifts to larger junction depths. The current increases as the alloy layer thickness decreases, since more light can then penetrate to the GaAs. The biggest increase in photocurrent occurs for thicknesses of 2μ or less. Figure 12 shows the photocurrent contributions from each of the 3 regions of the cell (0.5μ junction depth). The largest contribution comes from the top region (pGaAs), with minor contributions from the base and the depletion region (not shown). The $Ga_{1-x}Al_xAs$ contributes a few percent to the current, with a peak at a thickness of around 3000 Å. The total photocurrent becomes nearly constant for thicknesses less than 1000 Å.

Table 8 lists the measured short circuit currents of cells with various $Ga_{1-x}Al_xAs$ thicknesses and junction depths. The measured currents have been corrected for the contact area in order to better compare them with theory. In practice, the photocurrents depend upon the junction depth, the $Ga_{1-x}Al_xAs$ composition and thickness, the index and thickness of the antireflection coating, and the diffusion lengths in the base and diffused (pGaAs) region. The data of Table 8 show that: J_{AM0} depends weakly on junction depth as long as the substrate diffusion length is good; J_{AM0} improves slowly with decreasing $Ga_{1-x}Al_xAs$ thickness down to several microns, and improves more rapidly with decreasing thicknesses thereafter; the current is around 10% higher using "good" (high diffusion length) substrates compared to "poor" substrates; leaching is capable of improving the photocurrent considerably, probably by ensuring good diffusion lengths in the pGaAs region; large

photocurrents (high collection efficiency) can be obtained even with very large junction depths. All of these conclusions are in agreement with the theoretical calculations. Quantitatively, the measured photocurrents are about 10% lower than the computed ones (for "good" substrate parameters) shown in Figure 11. The discrepancy is probably due to a combination of non-optimized anti-reflection coatings, diffusion lengths slightly smaller than those used in the calculations, and possibly higher absorption coefficients of the actual $Ga_{1-x}Al_xAs$ layers compared to the assumed values (Figure 17), which were extrapolated in part from the GaAs absorption coefficient.

Electrical Characteristics

The open circuit voltage and fill factor are determined by the current-voltage characteristics of the solar cell in the dark. In theory, the dark current is the sum of (at least) two separate components: one due to injection of minority carriers from the pGaAs into the base and the other due to the recombination of holes and electrons within the depletion region. The injected current takes the form

$$J_{inj} = J_1[\exp(qV_j/kT) - 1] \tag{17}$$

while the recombination current takes the form

$$J_{rg} = J_2 \sinh (qV_j/2kT) \quad . \tag{18}$$

The recombination current dominates at low voltages and the injection current at higher voltages. A change in the slope of the ℓn J versus V curve should

occur, with slopes close to 2 at low voltages and close to 1 at higher voltages.

The measured I-V characteristics of several devices are shown in Figure 13. These data were taken by the V_{oc}-I_{sc} method, which eliminates series resistance effects. Nearly all devices show the expected break in slope, with values of 1.8 to 2.1 at low currents and 1.1 to 1.6 above 1-2 millamps/cm^2. The curve labelled 298 is typical of very high V_{oc} units, $V_{oc} \sim 0.98$-1.0 volt. The curve labelled 454 is typical of most devices made during this contract, having V_{oc}'s of 0.94 to 0.97. Device 64-3 is characteristic of units made with poor starting substrates. 336-4 typifies devices in which a high defect density was introduced during the external Zn diffusion. Finally, 46 shows the effect of a shunt resistance of about 10^5 ohms, which causes excess current at low voltages but isn't high enough to affect the V_{oc}.

The slopes of the ℓn J - V curves together with the extrapolated zero bias current J_0, the open circuit voltage, and the reverse current at -1 volt are given in Table 9. There is some correlation of V_{oc} with slope and reverse current; the highest V_{oc}'s are obtained when the reverse current is a few nanoamps and the high current slopes are 1.1-1.3. Devices with these parameters have only been obtained using high quality substrates, i.e. when the base diffusion length was known to exceed several microns.

Devices with V_{oc}'s in the 0.94-0.96 range are usually obtained with "moderate quality" substrates, diffusion lengths of 1-2 microns. The slopes are normally higher than in the best units, from 1.5 to 1.9, and the reverse currents also slightly higher.

Devices with V_{oc}'s of <0.92 are generally obtained from poor quality substrates (unleached) and the slopes are around 2 or above. Occasionally a low V_{oc} device is found with reasonably low A (slope) values and low reverse currents; in these cases the low V_{oc} is due to a small photocurrent; device 414 is an example of this. In other cases a very low shunt resistance (100's of ohms) results in poor voltage output. This was traced back to the Au-Zn or Ag-Zn contact sintering; both Au and Ag seem to amalgamate with GaAs and $Ga_{1-x}Al_xAs$ if the sintering temperature exceeds 500°C for more than a few seconds, causing shorts across the p-n junction. (The sintering temperature must be greater than 450°C for low contact resistance to be obtained.)

The parameter which correlates best with open circuit voltage is the extrapolated zero-bias current J_0. This current is a direct measure of the quality of the base. When J_0 is of the order of 10^{-16} amps/cm^2 or smaller, it is given by J_1:

$$J_0 = J_1 = q \frac{D_n}{L_n} \frac{n_i^2}{N_a} \left[\frac{(S_n L_n/D_n) \cosh (x_j/L_n) + \sinh (x_j/L_n)}{(S_n L_n/D_n) \sinh (x_j/L_n) + \cosh (x_j/L_n)} \right]$$
$$+ q \frac{D_p}{L_p} \frac{n_i^2}{N_d} \left[\frac{(S_p L_p/D_p) \cosh (H'/L_p) + \sinh (H'/L_p)}{(S_p L_p/D_p) \sinh (H'/L_p) + \cosh (H'/L_p)} \right] \qquad (19)$$
$$\approx q \frac{D_p}{L_p} \frac{n_i^2}{N_d}$$

while currents of 10^{-12} or more imply space charge layer recombination and J_0 is given by J_2:

$$J_0 = J_2 = \frac{2q\, n_i\, W\, (\pi/2)}{\sqrt{T_{po}\, T_{no}}\; q(V_d - V_j)/kT} \; . \qquad (20)$$

Low values of J_0, from 10^{-8} to 10^{-9} are generally accompanied by V_{oc}'s in the 0.8-0.9 range, 10^{-10} - 10^{-12} by V_{oc}'s of 0.9-0.95, and < 10^{-12} by higher V_{oc}'s. Variations of the slope A cause minor modifications to this trend of V_{oc} as a function of J_0.

Efficiency

The device efficiencies were measured using an Oriel xenon light source (1000 watt) as a solar simulator. The AM0 efficiencies of several units were measured at JPL using their solar simulator; these devices were used to calibrate the power input to all the cells. There are probably some differences between the JPL simulator spectrum and the xenon spectrum, but any resulting errors in the measured efficiencies should be minimized in this way.

The theoretical device efficiencies were calculated from the short circuit current calculations and the sum of the two dark current components. The efficiency bersus GaAlAs thickness for the conditions of Table 7 is shown in Figure 14. The efficiency increases slowly as the GaAlAs is made thinner in the range of 10 to 1 micron, increases more rapidly down to 2000 Å, and slowly again below this. The ultimate limit here of about 21% is determined by the loss due to light absorbed in the GaAlAs and the fact that most of the carriers generated in this layer are lost due to the higher recombination velocity at the GaAlAs surface. If this recombination velocity were lower, the ultimate AM0 efficiency of 24% could theoretically be reached.

Most of the devices made during the contract have been 12% (AM0) or better, with heavily defected or shunted devices being the main exceptions.

Table 10 lists a number of units for which the junction depth and GaAlAs thickness are known. Devices made on "good" substrates are normally a percentage point or more higher than devices made on "poor" substrates for otherwise equal conditions. The efficiency improves slowly with decreasing GaAlAs thickness down to around a micron and more rapidly thereafter, for otherwise equal conditions. The efficiency is affected much less by junction depth than origionally expected, almost surely because the electron diffusion length in all cases is considerably larger than the junction depth and at the same time interface recombination is not a problem. The weak dependence on junction depth is strong evidence that interface recombination is negligible.

It is certainly desirable to fabricate devices on high diffusion length substrates. A comparison of devices, 62 and 64, however, demonstrates that it is possible to produce good cells on poor substrates by a combination of "leaching" and deep junctions. The leaching allows fast-diffusing, lifetime-killing impurities such as Cu to be removed from the GaAs into the highly pure Ga-Al melt. The deep junction ensures that all the light will be absorbed in the high lifetime leached region instead of the low lifetime base region. (Of course, the diffusion length in the pGaAs must be larger than the junction depth for this scheme to work.) Further discussion of the benefits of leaching is given in the appendix.

Contact and series resistance were two other factors besides poor substrates limiting the measured efficiencies. Table 10 shows that most of the fill factors fell in the 0.77-0.78 range, others in the 0.74-0.75 range, and still others below this. These low fill factors were the result of

high series resistance, and the measured efficiencies would have been 0.5 percentage point higher in most cases if the series resistance were reduced. Much more attention should be paid to this point in the future.

Temperature Effects

One of the advantages of GaAs cells is their ability to operate efficiently at high temperatures. The realtive decrease in open circuit voltage is less than in lower bandgap devices, and the short circuit current increases with temperature.[2] As a result, efficiencies of 6% (AM1) at 300°C have been measured.[2]

The increasing photocurrent contributes substantially to the high efficiencies at elevated temperatures. The increasing currents are a result of the decreasing bandgap of GaAs (offset slightly by the decreasing bandgap of GaAlAs) and the improving minority carrier duffusion lengths in GaAs. The bandgap of GaAs varies as[5]

$$E_g = 1.522 - \frac{5.8 \times 10^{-4} T^2}{T + 300} \qquad (21)$$

This gives 1.437 eV at 294°K, 1.354 at 473°K, and 1.252 eV at 673°K. The shift in the absorption edge to longer wavelengths "gathers-in" more sunlight and increases the current accordingly.

The shift in the absorption edge of $Ga_{1-x}Al_xAs$ with temperature for $x = 0.73$ is shown in Figure 15. The shift is substantial for thick GaAlAs layers but is much less for thinner layers, as shown in Fig. 16. Therefore almost the full benefit of the shifting GaAs band gap can be obtained if the GaAlAs layer is very thin.

The increase in diffusion length with increasing temperature is due mainly to increasing minority carrier lifetimes.[6] These in turn could be due to a decreasing density of recombination centers and/or a decrease in the capture cross sections of these centers. Substantial improvements in minority carrier diffusion lengths with temperature have been reported by Vilms and Spicer,[6] and they can be seen by the increased spectral response between 1.5 and 2.0 eV in Figures 15 and 16.

The important device parameters (I_{sc}, V_{oc}, FF, η) of several cells were measured at 1 sun intensity ($\sim$134 mW/cm^2) using the xenon solar simulator. The units were mounted on a copper strip along with a heating supply and a thermocouple. The measurements were made in a vacuum chamber with the light entering through a sapphire window.

Figure 17 shows the J_{sc}, V_{oc}, FF, and efficiency from room temperature to 250°C for one device with a 11μ thick GaAlAs layer and a 3.5μ junction depth. Both the V_{oc} and FF decrease with temperature, while the J_{sc} increases. The net result is that the efficiency is usually a slowly changing function of temperature below 100°C and decreases more rapidly thereafter (Fig. 18). In some devices, such as that of Figure 17, the relative changes in V_{oc} and J_{sc} can actually produce a slight increase in η with T.

The major factor diminishing the efficiency with temperature is the open circuit voltage, just as it is in Si cells. The higher bandgap of GaAs, however, results in a smaller relative decrease in V_{oc} compared to Si, producing good efficiencies at high temperatures. In the single exponential approximation for the dark current, the V_{oc} varies as:

$$V_{oc} = A \frac{kT}{q} \ln\left(\frac{I_{ph}}{I_o} + 1\right) \tag{22}$$

where A is the slope of the ln J-V characteristic and I_o is the dark current extrapolated to zero bias. The variation of the photocurrent I_{ph} with temperature has already been discussed. The dark current term was given in (19) or (20):

$$I_o \propto n_i \text{ or } n_i^2 \tag{23}$$

where

$$n_i^2 = N_c N_v e^{-Eg/kT}$$
$$= 4.26 \times 10^{30} T^3 e^{-Eg/kT} \tag{24}$$

for GaAs. The bandgap variation was given in eq. (18). The intrinsic carrier density n_i varies exponentially with temperature, and the V_{oc}, related to the log of I_o, varies (approximately) linearly as a result.

Device Fabrication.

The GaAlAs-GaAs wafers are normally given a post-growth Zn diffusion to increase the doping level at the surface. After the wafers are removed from the diffusion tube, they are covered on the growth side with a layer of photoresist and black (apiezon) wax. The back side of the cell is then lapped with 3 micron grit to remove the diffusion from the back, followed by etching for 30 seconds in H_2O_2:NH_4OH. After removing the wax the photoresist from the growth side, the wafer is loaded into the evaporator and 5000 Å of Au-Ge-Ni are applied to the back; this contact is then sintered at 500°C for 5 minutes in pure He. The cell is then mounted onto a metal mask holder and about 5000 Å

of Ag-2% Zn are evaporated onto the growth side in the desired contact grid design.

Following the grid metallization, the unit is re-annealed at 450-475°C for 2 minutes, and then re-covered with a thin photoresist layer and mounted on a metal block for dicing. All 4 edges are sawed off and the remainder cut into 4 pieces. After removing the photoresist, each piece is bonded to a TO-5 header with either conducting silver epoxy or electroplated In. A 3 mil Au wire is bonded to the grid metalization either by "thermo-compression bonding" or with silver epoxy.

The upper surface and bottom edges of the mounted device are covered with black wax, and the unit is etched in $9H_3PO_4:1HNO_3$ to remove saw damage and other edge problems that could cause low shunt resistances. The black wax is removed with trichloroethylene and the sample is carefully cleaned in solvents to remove all wax and other organics. The header is then mounted onto a Cu plate, loaded into an evaporation chamber, and covered with about 750 Å of SiO or Al_2O_3 as an anti-reflection coating. This finishes the fabrication process.

Generally, the 4 devices from a given run exhibit significant differences in behavior. One or two of the cells may have considerably higher open circuit voltages and fill factors than the others. It appears that this may be due to problems of the Ag-Zn contact. This metallurgy does not adhere well to GaAlAs, and can cause serious shunt resistance problems if the contact is sintered for too long or at too high a temperature. (The shunt resistance problem is much worse with Au-Zn than with Ag-Zn.)

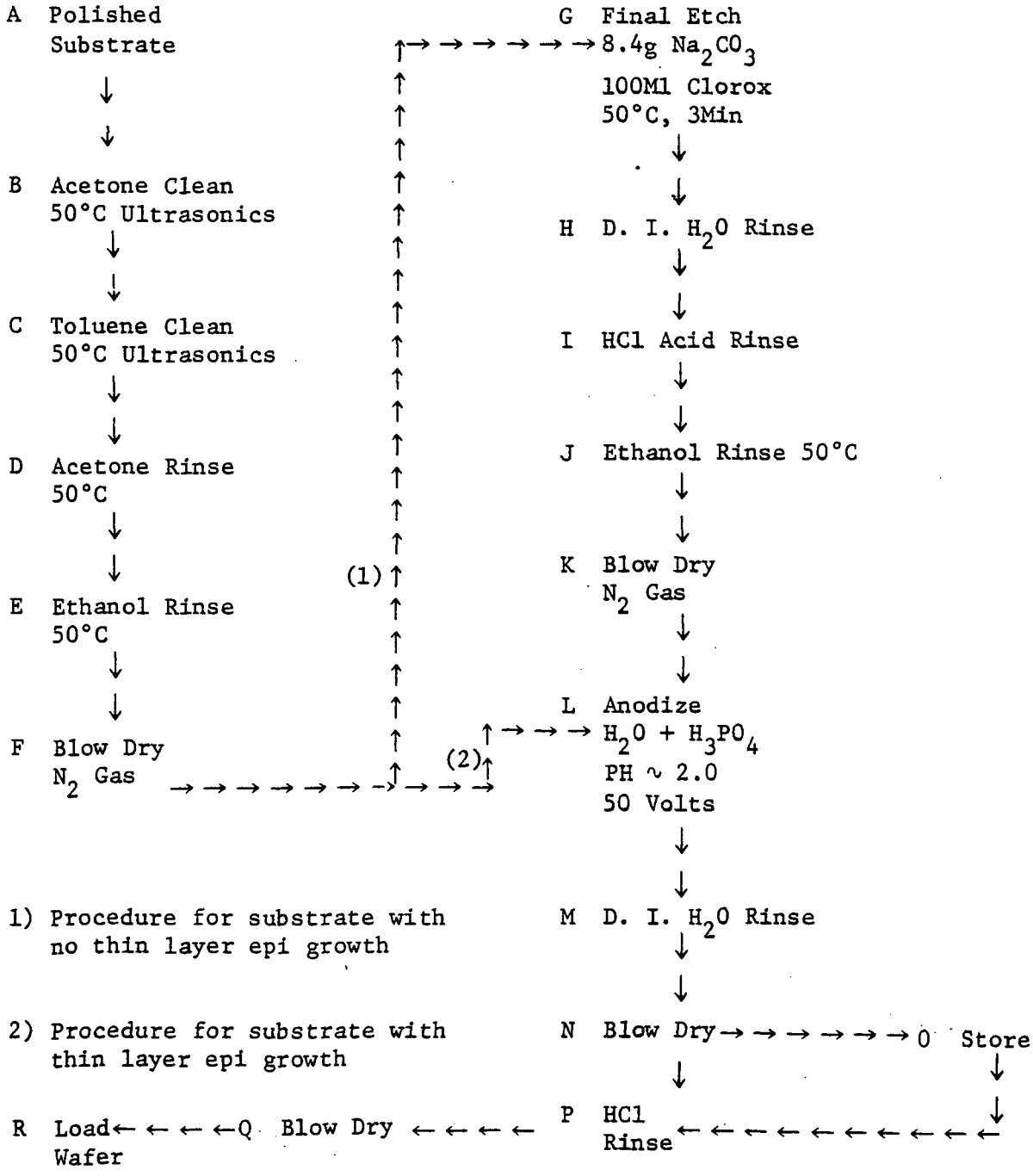
The major deviation between cells of the same run is in the short circuit current. Table 11lists the measured parameters of two cells.

The first set shows considerable differences between V_{oc}'s and FF's and not too much between J_{sc}'s. The second set shows more deviation between FF's and J_{sc}'s. The second set is typical of most runs. The variations in J_{sc} have been traced back to a considerable variation in quantum efficiency over the surface of the fabricated wafer. Figure 14 shows a particularly bad example. A He-Ne laser spot (6328 Å) was stepped along the surface and the photocurrent output was recorded as shown. Variations of 250% in quantum efficiency are observed. Since the GaAlAs is transparent at this wavelength, changes in its thickness are not responsible, nor are differences in surface reflectivity. The response can be either high or low near the metal contact, eliminating that as the major problem. Either the starting substrates are very non-uniform (by an order of magnitude) in their lifetimes or some gross non-uniformities are introduced during the growth or diffusion process. If poor starting substrates are the cause, leaching could be very beneficial in overcoming the problem.

References

1. H. J. Hovel and J. M. Woodall, Conf. Rec. 10th IEEE Photovoltaics Specialists Conf., Palo Alto, Nov. 1973; pg. 25.
2. H. J. Hovel and J. M. Woodall, J. Electrochem. Soc. 120, 1246 (1973).
3. H. J. Hovel, J. M. Woodall, and W. E. Howard, 1972 Symposium on GaAs and Related Compounds, Proceedings, Boulder, Sept. 1972; pg. 205.
4. M. P. Thekaekara, Solar Energy 14, 109 (1973).
5. M. P. Panish and H. C. Casey, Jr. J. Appl. Phys. 40, 163 (1969).
6. J. Vilms and W. E. Spicer, J. Appl. Phys. 36, 2815 (1965).
7. M. P. Panish and M. Illegems, Progress in Solid State Chemistry Vol. 7. Ed Reiss and McCouldin Pergamon Press (1972).

Table 1. Wafer Preparation Steps



1) Procedure for substrate with no thin layer epi growth

2) Procedure for substrate with thin layer epi growth

Table 2. Melt Compositions, Layer Compositions, Layer Thicknesses for Ga-Al-As Melts Saturated with GaAs at 900°C

Weight Al (in gms.) per gm of Ga	X in $Ga_{1-x}Al_xAs$ Layer	Thickness (in micron per gm. Ga, °C cooling and cm^2 of substrate area
0.27×10^{-3}	0.1	3.0
0.6×10^{-3}	0.2	2.6
1.02×10^{-3}	0.3	2.3
1.56×10^{-3}	0.4	1.9
2.31×10^{-3}	0.5	1.6
3.42×10^{-3}	0.6	1.2
5.26×10^{-3}	0.7	0.93
8.97×10^{-3}	0.8	0.62
20.4×10^{-3}	0.9	0.31

Table 3. Flow Diagram for LPE Growth

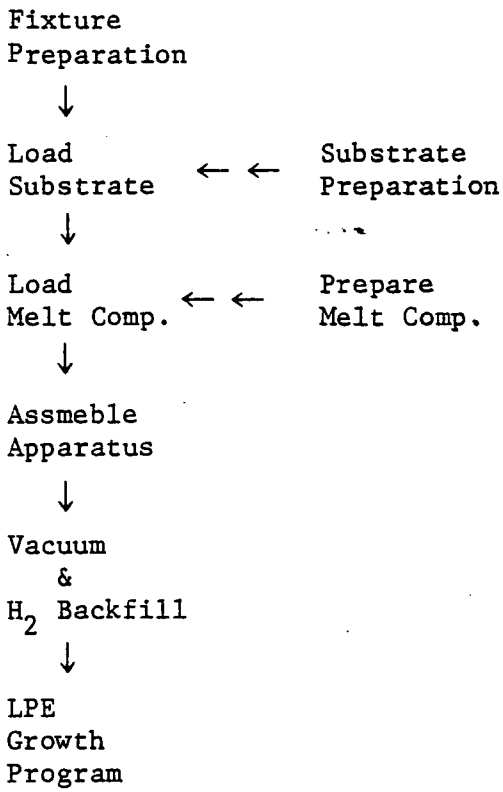


Table 4. List of Runs and Growth Parameters

SCB Run#	W Ga gms	W Al mg	X*	D μ	C_{zn} mg/g	χ_j μ	T_g	ΔT °C	Z_n Diff	Leach time	Growth Sch Fig	Up Heat Temp	Fixture #	Sub #	Comments
1	1.8	13	0.75	1.8	7.2	1.1*	904	1.5	-	10'	2	-	1	PU-88	
2	1.8	12.6	0.75	1.6	7.2	1.2	909	1.75	$\frac{600°C}{0.5hr}$	"	2	-	1	"	
3	1.0	13.2	0.83	1.6	13	1.2	920	5	"	"	2	-	1	"	
4	1.0	13.2	0.83	1.6*	13	1.2*	910	5	"	60'	2	-	1	"	
5	1.0	13.0	0.83	1.6*	13	1.2*	920	5	"	70'	2	-	1	"	
6	1.0	13.1	0.83	1.6*	13	1.2*	918	5	"	70'	2	-	1	"	
7	2.0	14.7	0.75	3.2*	7.2	1.2*	900	2	"	60'	2	-	3	"	
8	2.0	14.4	0.75	3.7	7.2	0.8	904	1.7	"	70'	2	-	3	"	
9	2.0	14.8	0.81	3.8	7.2	1.2	803	RT	"	60'	2	-	3	"	0.025" x 0.3" x 0.5" volume of melt cooled to room temperature
10	5.0	64.9	0.86	0.8*	12	1.2*	850	1	$\frac{680°C}{15'}$	60'	2	-	2	424	0.060 gms Ge in melt
11	5.0	150	0.93	1.5*	12	1.2*	850	2	"	60'	2	-	2	"	0.012" x 0.5" volume of melt cooled to room temperature
12	2.0	20.9	0.85	-	10	1.2*	810	RT	-	60'	2	-	2	"	

*Calculated Values

Table 4. (cont.)

13	2.0	14.8	0.75	1.6*	7.2	1.2*	900	1	$\frac{680°C}{15'}$	60'	2	-	3	424	
14	1.0	13.2	0.83	-	12	-	904	3	-	10'	2	-	1	PU-88	No growth Wafer dislocated during run
15	1.12	12.8	0.82	0.9*	12	1.2*	902	2.2	-	10'	2	-	1		
16	1.12	13.0	0.83	0.9*	12	1.2*	903	2.5	-	60'	2	-	1	"	
17	2.0	14.6	0.75	3.2*	7.2	1.2*	895	2	-	60'	2	-	3	"	Anodized layer not removed before loading substrate
18	3.0	21.9	0.75	3.5	7.2	1.6	901	1	$\frac{680°C}{15}$	60'	2	-	3	"	Ga bake then Al & Zn added to melt
19	3.0	21.8	0.75	7.9	7.2	1.3	898	1	$\frac{680°C}{15}$	60'	2	-	3	424	Ga bake then Al & Zn added to melt
20	5.0	64.9	-	-	-	-	853	-	-	16hrs	2	-	2	424 P-Si-97	Leaching experiment
21	5.0	64.9	-	-	-	-	853	-	-	60'	2	-	2	424 P-Si-97	Leaching experiment
22	5.0	64.9	-	-	-	-	850	-	-	0	4	-	2	424 P-Si-97	Leaching experiment
23	-	-	-	-	-	-	-	-	-	-	-	-	-	424 P-Si-97	Control wafers
24	3	60	0.9	1.0*	20	1.5*	903	1	-	60'	2	-	2	424	Al, Zn, and GaAs dropped into melt

Table 4. (cont.)

25	3.0	60	0.9	1.0*	20	1.5*	893	1	-	60'	2	-	2	424	Same as SCB 24
26	5.0	100	0.9	-	20	-	897	1	-	60'	2	-	2	424	Al drop into melt failed substrate dissolved
27	5.0	100	0.9	1.0*	20	1.5*	920	1	-	60'	2	-	2	424	Drop Al and Zn GaAs source in substrate holder
28	5.0	63.6	0.85	-	-	-	857	-	-	16hrs	3	-	2	424 P-Si-97	Al drop, GaAs source bar Leaching experiment
29	1.2	17.6	0.85	-	-	-	895	-	-	18hrs	3	-	2	424 P-Si-97	Al, GaAs source bar together Leaching Experiment
30	1.5	22.3	0.85	-	-	-	900	-	-	0	3	-	2	424 P-Si-97	Al, GaAs source bar together Leaching experiment
31	1.5	22.3	0.85	-	-	-	903	-	-	60'	3	-	2	424 P-Si-97	" " " "
32	1.5	22.1	0.85	-	-	-	902	-	-	13'	3	-	2	424 P-Si-97	" " " "
33	1.46	21.5	0.85	-	-	-	898	-	-	0	3	-	2	424 P-Si-97	No melt contact control wafers
34	1.52	22.3	0.85	-	-	-	898	-	-	12.7hrs	3	-	2	424 P-Si-97	wafers made melt contact
35	1.50	22.0	0.85	-	-	-	898	-	-	0	3	-	2	424 P-Si-97	wafers made melt contact
36	1.43	21.0	0.85	-	-	-	897	-	-	2.5hrs	3	-	2	424 P-Si-97	

Table 4. (cont.)

37	1.52	22.4	0.85	1.5*	14.4	1.3*	896	2	-	60'	2	-	2	424	Al and GaAs source bar in separate positions in substrates
38	1.94	28.6	0.85	1.9*	14.4	1.3*	894	2	-	60'	4	-	2	424	First run with Growth Schedule of Fig. 5
39	1.94	28.6	0.85	1.9*	14.4	1.3*	893	2	800°C / 10'	60'	4	-	2	424	
40	1.96	18.9	0.85	2.2	14.4	3.4	898	2	700°C / 15'	60'	4	-	2	424	
41	1.93	28.4	0.85	2.1	14.4	3.1	911	2	-	30'	5	15°C	2	424	
42	4.6	67	0.85	1.0	14.4	1.4	893	1	-	60'	5	-	2	424	Zn drop end of leaching time
43	1.96	28.8	0.85	2.2	-	0	890	2	704° / 30'	60'	5	-	2	424	No Zn doping during growth Zn diffusion, $x_j = 0$
44	1.9	28	0.85	1.2	1.4	1.0	895	1	800° / 10'	60'	5	-	2	424	After Zn diffusion $x_j = 3.1\mu$
45	1.86	27.4	0.85	1.1*	1.4	0.5*	906	1	700° / 2'	30'	5	15°	2	424	
46	1.9	28.1	0.85	1.1	1.4	1.1	895	1	-	60'	5	10	2	424	
47	2.0	29.4	0.85	0.6	14.4	3.1	895	0.5	-	10'	4	-	2	424	
48	1.88	27.6	0.85	0.6*	14.4	2.9	895	0.5	800°C / 5min	10'	4	-	2	424	

Table 4. (cont.)

49	1.9	59	0.95	0.2*	14.4	3.1	893	0.5	-	10'	4	-	2	424	Poor growth scratches
50	1.9	23**	0.85	0.5*	-	6*	850	1.5/1.0	-	60'	4	-	2	424	19mg Ge in melt 1 No Al χ^*_j = 6μ poor growth
51	1.9	23**	0.95	0.5*	-	4*	85	1.0/1.0	-	60'	4	-	2	424	19 mg Ge, No Al in Melt 1 ** = melt 2
52	1.9	56	0.85	0.2*	14.4	3.1*	896	0.5	-	10'	4	-	2	424	poor growth scratches
53	1.9	28	0.85	0.6*	14.4	3.1*	895	0.5	-	10'	4	-	3	424	poor growth scratches
54	1.97	28.9	0.85	3.0	14.4	3.1*	894	0.5	-	10'	4	-	3	424	No melt wiping - scratches
55	1.93	28.4	0.85	2.1	14.4	3.1	903	0.5	-	10'	4	-	3	424	poor growth - scratches
56	1.85	27.4	0.85	0.6*	14.4	3.1*	896	0.5	-	10'	4	-	2	424	poor growth
57	1.96	28.9	0.85	-	14.4	-	916	0.5	-	10'	4	-	2	424	poor growth Not enough source bar
58	1.9	28.7	0.85	0.6*	14.4	3.1	896	0.5	-	10'	4	-	2	424	
59	1.99	29.2	0.85	0.7	14.4	3.1*	897	0.5	-	20'	4	-	2	424	hold 20 min constant temp. before substrate contact melt
60	2.35	28.7	0.85	0.75	14.4	3.1*		0.5	-	20'	4	-	2	424	same as 59

Table 4. (cont.)

61	1.97	28.9	0.85	0.7	14.4	3.1*	897	0.5	-	10'	4	-	2	B-2-72	New substrates
62	1.94	28.5	0.85	0.7*	14.4	3.1*	896	0.5	800°C / 2'	10'	4	-	2	424	good run except for occasional non wetting
63	1.9	27.8	0.85	0.7*	14.4	3.1*	894	0.5	800°C / 2'	10'	4	-	2	424	
64	1.9	27.9	0.85	0.7*	14.4	3.1*	897	0.5	-	10'	4	-	2	B-2-72	
65	1.9	28.8	0.85	-	1.4	-	900	0.5	-	20'	5	2.5°	2	B-2-72	Substrate dislocated from holds during run
66	1.95	28.7	0.85	0.8	1.4	1.1*	903	0.5	-	60'	4	-	2	B-2-90	
67	1.95	28.6	0.85	0.7*	1.4	1.1*	898	0.5	-	60'	4	-	2	B-2-90	
68	2.0	61	0.93	0.8	1.4	-	894	0.5	-	10'	4	-	3	424	GaAs quench melt
69	2.0	61	0.93	0.8	1.4	-	893	0.5	-	60'	4	-	3	424	GaAs quench melt
70	2.0	33.9	0.9	2.5	1.4	3.5**	847	1.5 / 1.5	-	60'	4	-	3	424	19 mg Ge No Al melt 1 ** - χ_j = 3.5μ Ge doped GaAs
71	2.0	34.6	0.9	1.0	1.4	2.1	848	1.5 / 1.5	-	60'	4	-	3	424	19 mg Ge, No Al melt 1
72	2.0	-	0	2-4	-	9.5**	848	2	-	60'	4	-	3	424	** - 19 mg Ge in melt

Table 5. Some Device Characteristics of Cells Tested

Cell	Spectral Response Low hν	High hν	Cut Off eV	A fact.	Leakage at -1 volt.	V_{oc}	FF	I_{sc} Uncor. Ma.	η	Area cm^2
2	Good	Good	2.6	2.9	8.9μ	.883		3.05		
3	Good	Good	2.6	>>3	8.9μ	.902	.25	3.05		
4	Poor	OK	2.6	>>3	86μ	.877	∿.5	3.6		
5	Good	OK	2.6	1.95	15n	.932	∿.7	3.00		
6	Good	Good	2.55	1.2	19n	.865	<.25	1.55		
7	-	-	-	-	-	.17	.25	0.7		
8	Good	Good	2.5	>3	3.6μ	.955	.75	3.1		
9.	Fair	Fair	2.65	2	19n	.940	.68	3.75		
15	Fair	Good	2.7	2.0	.53μ	.965	.75	2.10		.137
16	Good	Good	2.6	2.25	1n	.961	.74	1.81		1.28
39	Fair	Fair	2.4	2.05	13n	-	-	-		
40	Good	Drop Off	3.0	2.25	22n	.968	-	2.2		
41	Good	Drop Off	2.8	2.4	49n	.941	-	1.7		
43	Poor	Drop Off	3.0	-	.1μ	.955	.50	1.7		
44	Fair	Very Poor	2.6	2.0	.17μ	-	-	-		
46	Same as 287	Very Good	>3	2.5-3	2.5μ	.967	.722	2.30		
47	Good	Slow Drop	>3	>>3	2.4n	.965	.5	1.27		
62	Good	Drop Off	2.9-3	2	16n	.978	.795	3.76	14.65	.15
63	Good	Drop Off	2.8-3	-	-	.97	-	9.6		
64	Good	Drop Off	>3	2.24	.86μ	.97	.72	2.66		
66	Poor	Good	>3	-	-	.864	.6	1.28		
68	Poor	Poor	2,8-3	-	-	.450	-	.131		
70	Poor	Bad	>3	2.1	2.4μ	.83	-	.605		
71	Good	Poor	>3	-	-	.797	-	1.72		
72	-	Very Poor	>3	-	-	.650	-	.36		

Table 6. Leaching Experimental Results

Sample #	Carrier Conc. (electrons per cc)	Leaching Time in Hours			
		Control	0*	2.5	12.7
424L	$0.5 - 1.0 \times 10^{18}$	0.6	-	-	0.7
P - Si - 97	$1-2 \times 10^{18}$	0.34	-	0.48	0.89
P - U - 107 **	2.4×10^{17}	0.38	-	-	-
P - Sn - O - 108**	1.65×10^{17}	0.42	-	-	-

Hole diffusion length in microns for several GaAs samples

* melt contact followed by immediate return to room temperature

** Samples to test effect of oxygen in GaAs on hole diffusion lengths

Table 7. Parameters Used in Computer Calculations

$Ga_{1-x}AlAs$	pGaAs	nGaAs
$N_a = 2x10^{19}$ cm^{-3}.	$N_a = 2x10^{19}$ cm^{-3}.	$N_d = 6x10^{17}$ cm^{-3}.
$S_a = 10^6$ cm/sec.	$S_g = 10^4$ cm/sec.	
$D_a = 0.74$ cm^2/sec.	$D_g = 32.4$ cm^2/sec.	$D_p = 5.15$ cm^2/sec.
$L_a = 0.27$ micron.	$L_g = 1.8$ micron.	$L_p = 1.96$ mic.
$T_a = 1x10^{-9}$ sec.	$T_g = 1x10^{-9}$ sec.	$T_p = 7.46x10^{-9}$.

Table 8. Measured Short Circuit Currents, AM0, 300°K.

Device	D(GaAlAs) (μm)	x_j (μm)	J_{AM0}	Substrate
288-2	14	0.8	21.2	Good
287-2	5.5	0.8	22.7	Good
449-1	5.5	0.8	20.7	Poor
SCB46	0.6	1.1	24.3	Poor
452-3	2-4	1.8	23.6	Poor
453-3	2-4	1.8	22.8	Poor
454-3	2-4	1.8	24.7	Poor
289-3	16	2.7	21.3	Good
323-3	2-4	2.8	22.6	Good
335-2	11	2.8	22.4	Good
SCB64-3	0.6	3.0	22.3	Poor
SCB62-1	0.6	3.0	25.0	Poor, Leached

Table 9. Dark Current Parameters, 22°C

Dev.	Slope	Range mA/cm^2	I(-1v) amps	J_0 $amps/cm^2$	V_{oc} volt
298(1-2)	1.95	10^{-2}-1	$<1 \times 10^{-9}$		
	1.2	>5		2.9×10^{-16}	.98 - 1.0
289(3)	2.0	10^{-2}-0.5	3.5×10^{-9}		
	1.1	>10		1.86×10^{-17}	.97 - .98
454(3)	2.1	10^{-2}-1.5	38×10^{-9}	5.16×10^{-13}	.96 - .97
	1.55	>3			
46	R_{sh} high	10^{-2} to 5	233×10^{-9}		
	1.20	>5		5.32×10^{-16}	.953
453(3)	2.00	$>10^{-1}$	6.3×10^{-9}	1.89×10^{-10}	.93 - .95
312(1)	2.00	10^{-2}-3	3.1×10^{-9}		
	1.60	>5		2.14×10^{-12}	.940
446-1	R_{sh} high	<10	9.5×10^{-6}		
	2.1	>10		7.9×10^{-10}	.910
64(3)	2.02	10^{-2}-1	80×10^{-9}		
	1.50	>5		9.4×10^{-13}	.909
414(1)	2.05	$>10^{-2}$	48×10^{-9}	5.38×10^{-10}	.862
336(4)	1.80	<10	46×10^{-9}		
	2.50	>10		6.78×10^{-8}	.820

Table 10. Solar Cells, 300°K AMO Efficiency (contact area corrected)

$pGa_{1-x}Al_xAs$-pGaAs-nGaAs

Device	D (μm)	x_j (μm)	V_{oc} (volt)	FF	η (%)	Substrate
288(2)	14	0.8	.960	.812	11.9	Good
287(2)	5.5	0.8	.950	.779	12.2	Good
449(1)	5.5	0.8	.955	.800	11.8	Poor
SCB46	0.6	1.1	.953	.744	12.5	Poor
SCB15	1.8	1.1	.960	.788	11.9	Poor
SCB16	1.8	1.4	.958	.751	10.5	Poor
452-3	2-4	1.8	.962	.752	12.6	Poor
453-3	2-4	1.8	.955	.744	12.0	Poor
454-3	2-4	1.8	.962	.772	13.4	Poor
289-3	16	2.7	.970	.743	11.3	Good
335-2	11	2.8	.946	.796	12.2	Good
323-3	2-4	2.8	.956	.785	12.3	Good
SCB64	0.6	3.0	.909	.682	10.2	Poor
SCB62	0.6	3.0	.980	.802	14.5	Poor, Leached
298D1-2	11	3.5	.980	.807	12.1	Good

Table 11. Differences between cells from same run.

Cell #	V_{oc} (volt)	FF	J_{sc} (mA/cm^2)	η
454-1	.942	.782	22.99	13.1
-2	.980	.788	21.86	13.06
-3	.972	.773	23.63	13.7
-4	.996	.789	22.53	13.7
335-1	.957	.776	19.86	10.94
-2	.946	.796	21.94	12.26
-3	.941	.752	21.96	11.53
-4	.931	.703	20.98	10.19

Figure Captions

Fig. 1. The three apparatus used for the LPE growth of solar cells.

Fig. 2. The time-temperature program for LPE growth with no pre-cooling. See text for explanation.

Fig. 3. The time-temperature program for leaching experiments. See text for explanation.

Fig. 4. The time-temperature program for LPE growth with pre-cooling. See text for explanation.

Fig. 5. The time-temperature program for LPE growth with etch back. See text for explanation.

Fig. 6. Energy band diagram in equilibrium.

Fig. 7. Absorption coefficients.

Fig. 8. Spectral responses for decreasing $Ga_{1-x}Al_xAs$ thickness. Parameters of Table 7.

Fig. 9. Measured spectral responses for several $Ga_{1-x}Al_xAs$ thicknesses. 1: $D = 5.5\mu$ ($x_j = 0.8\mu$); 2: $D = 1.8\mu$ ($x_j = 1.1\mu$); 3: $D = 0.6\mu$ ($x_j = 1.1\mu$).

Fig. 10. Measured spectral responses for several junction depths. 46: $x_j = 1.1\mu$; 62: $x_j = 3.0\mu$. $Ga_{1-x}Al_xAs$ thickness = 0.6μ.

Fig. 11. Short circuit photocurrent. Parameters of Table 7.

Fig. 12. Short circuit photocurrent contributions from different regions of the cell. $x_j = 0.5\mu$. Parameters of Table 7.

Fig. 13. Measured current-voltage characteristics of several devices.

Fig. 14. Efficiency at AM0, parameters of Table 1. $x_j = 0.5\mu$.

Fig. 15. Variation of $Ga_{1-x}Al_xAs$ bandgap with temperature, thick $Ga_{1-x}Al_xAs$ layer.

Fig. Capts. Cont'd.

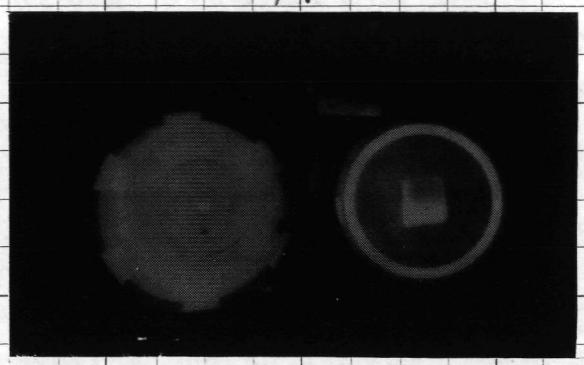
Fig. 16. Variation of $Ga_{1-x}Al_xAs$ bandgap with temperature, thin $Ga_{1-x}Al_xAs$ Layers.

Fig. 17. Device parameters under 134 mW xenon light.

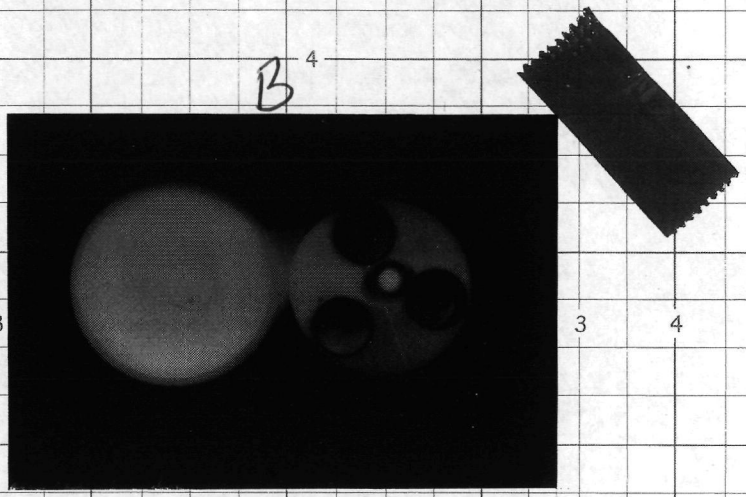
Fig. 18. Measured efficiencies under 134 mW xenon light.

Fig. 19. Quantum efficiency variations at 6328 Å. The numbers are in units of 10^{-1} milliamps.

A



B



C

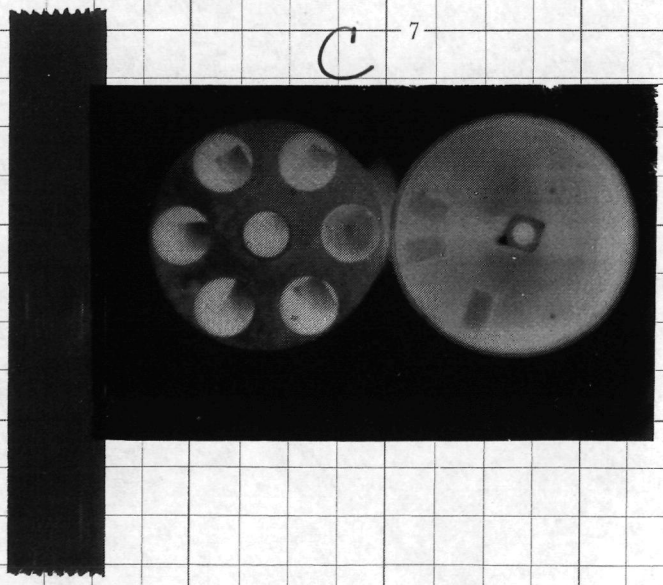


FIGURE 1

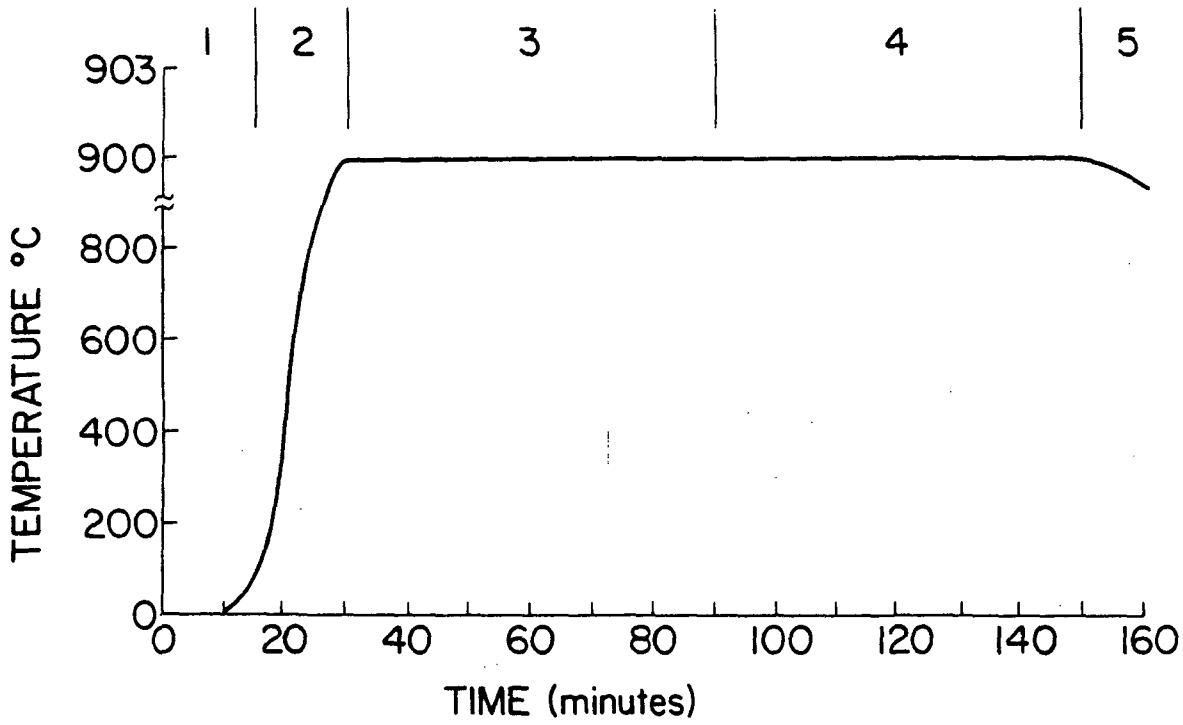

1
2
3
4
5
903
900
800
600
400
200
0
TEMPERATURE °C
0
20
40
60
80
100
120
140
160
TIME (minutes)

Figure 2

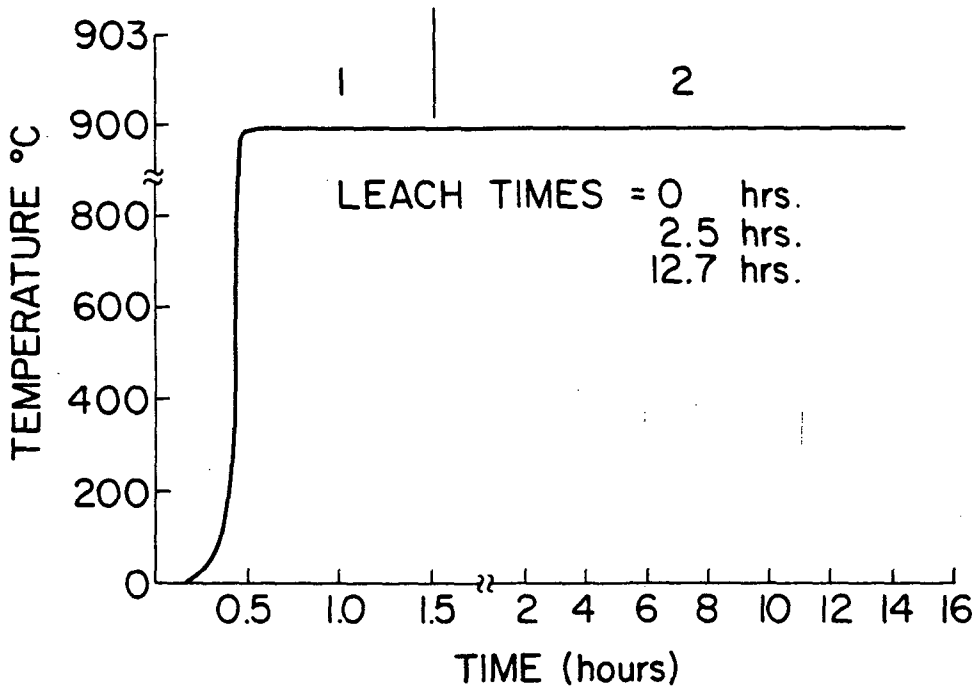

903
900
800
600
400
200
0
TEMPERATURE °C
1
2
LEACH TIMES = 0 hrs.
2.5 hrs.
12.7 hrs.
0.5
1.0
1.5
2
4
6
8
10
12
14
16
TIME (hours)

Figure 3

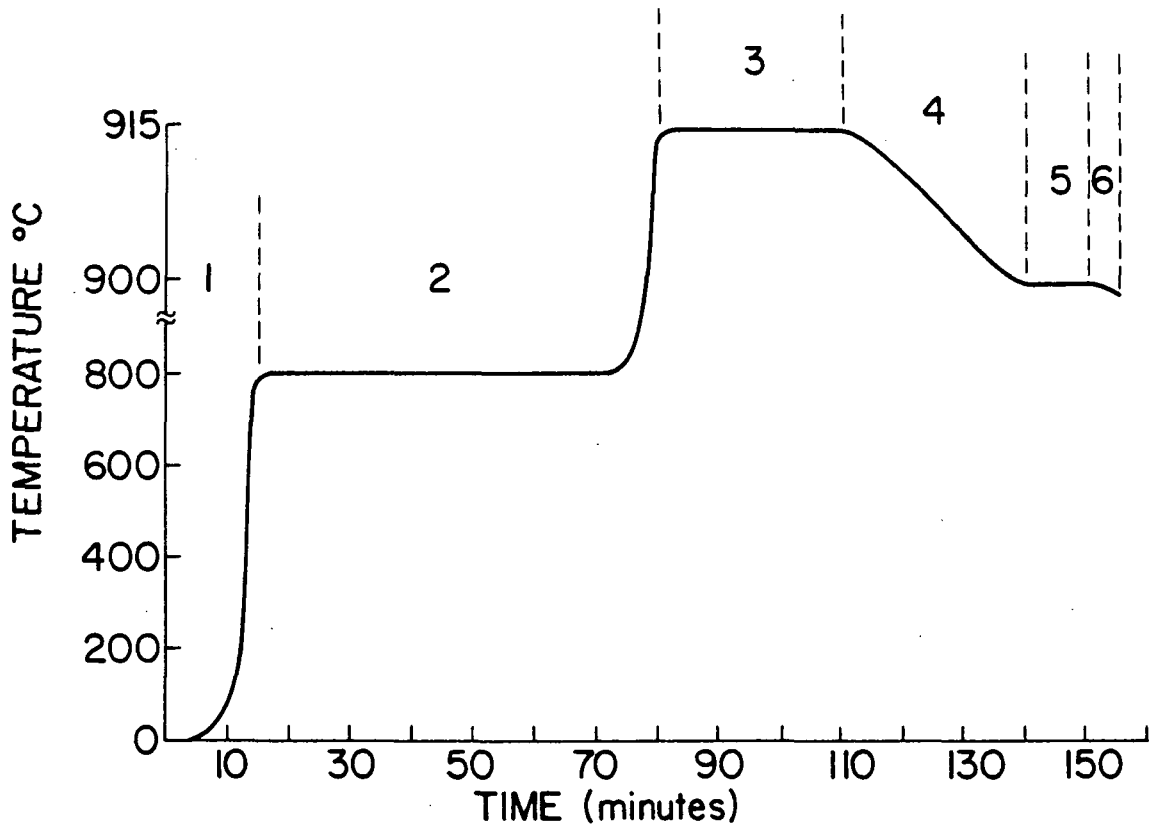

TEMPERATURE °C
915
900
800
600
400
200
0
1
2
3
4
5
6
10
30
50
70
90
110
130
150
TIME (minutes)

Figure 4

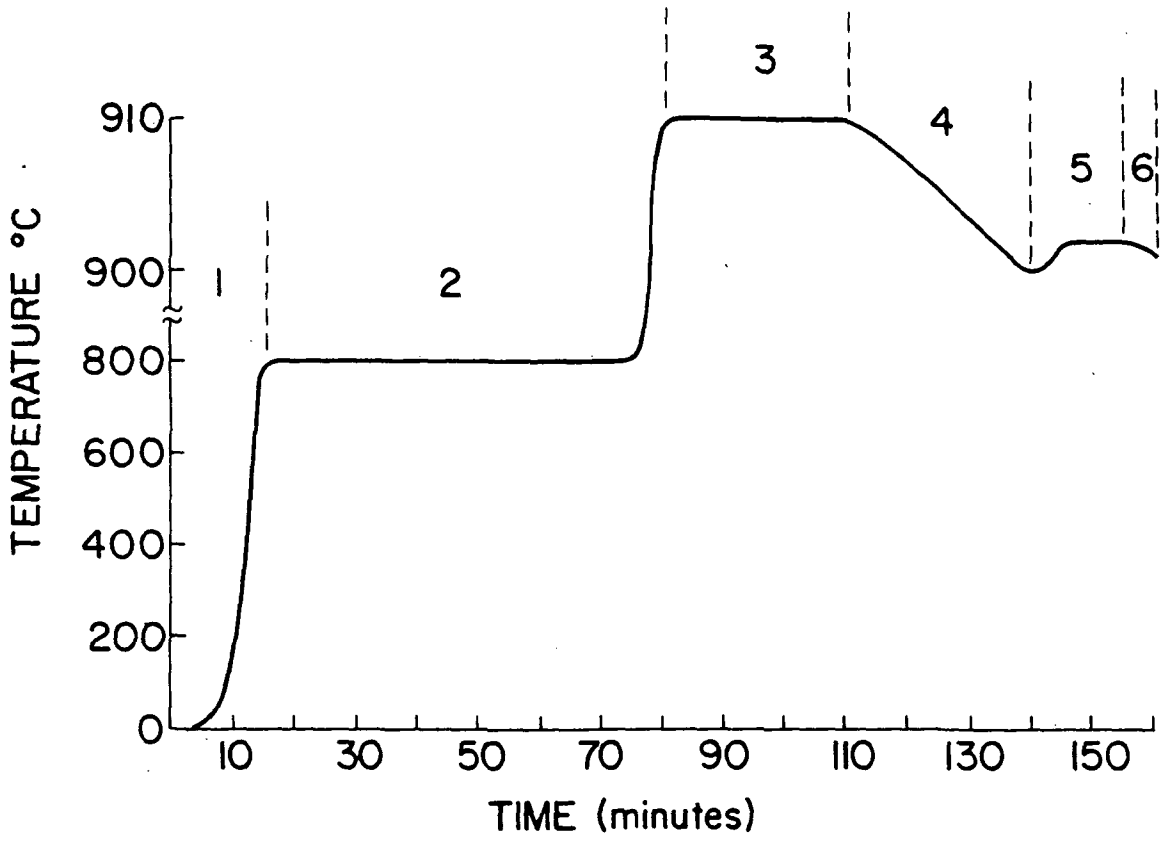

TEMPERATURE °C
910
900
800
600
400
200
0
1
2
3
4
5
6
10
30
50
70
90
110
130
150
TIME (minutes)

Figure 5

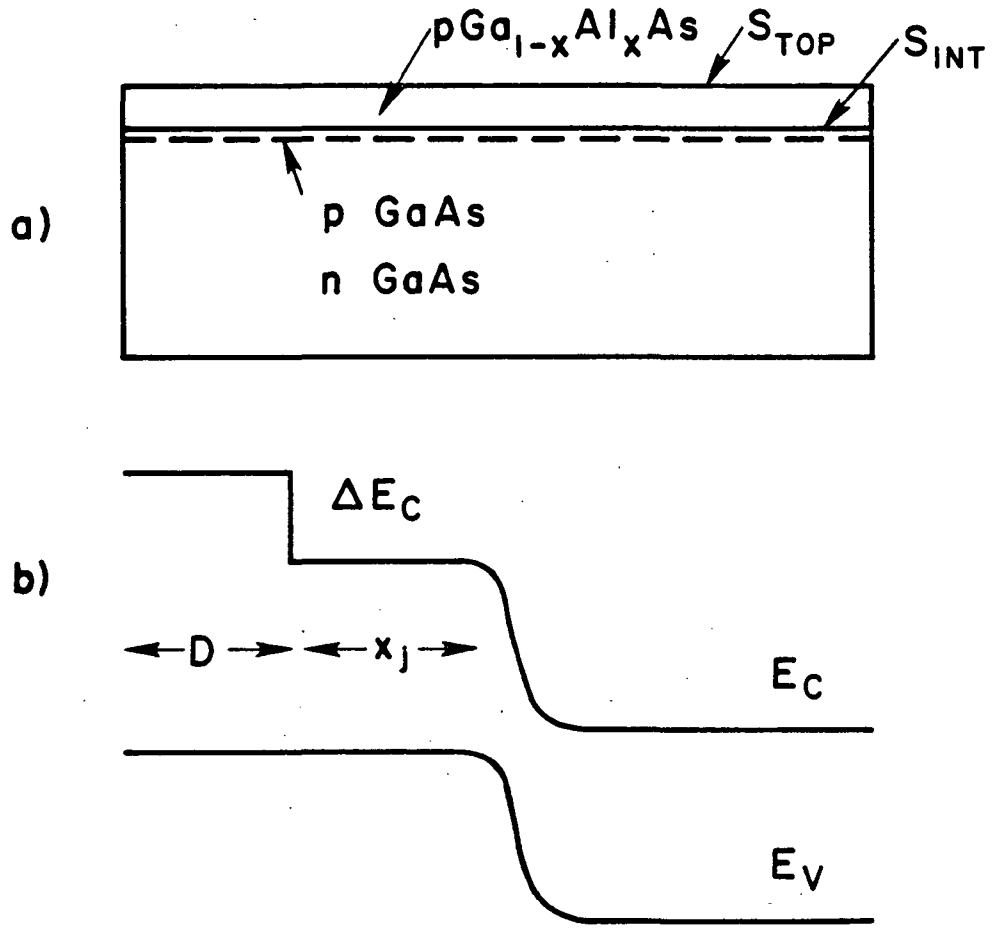
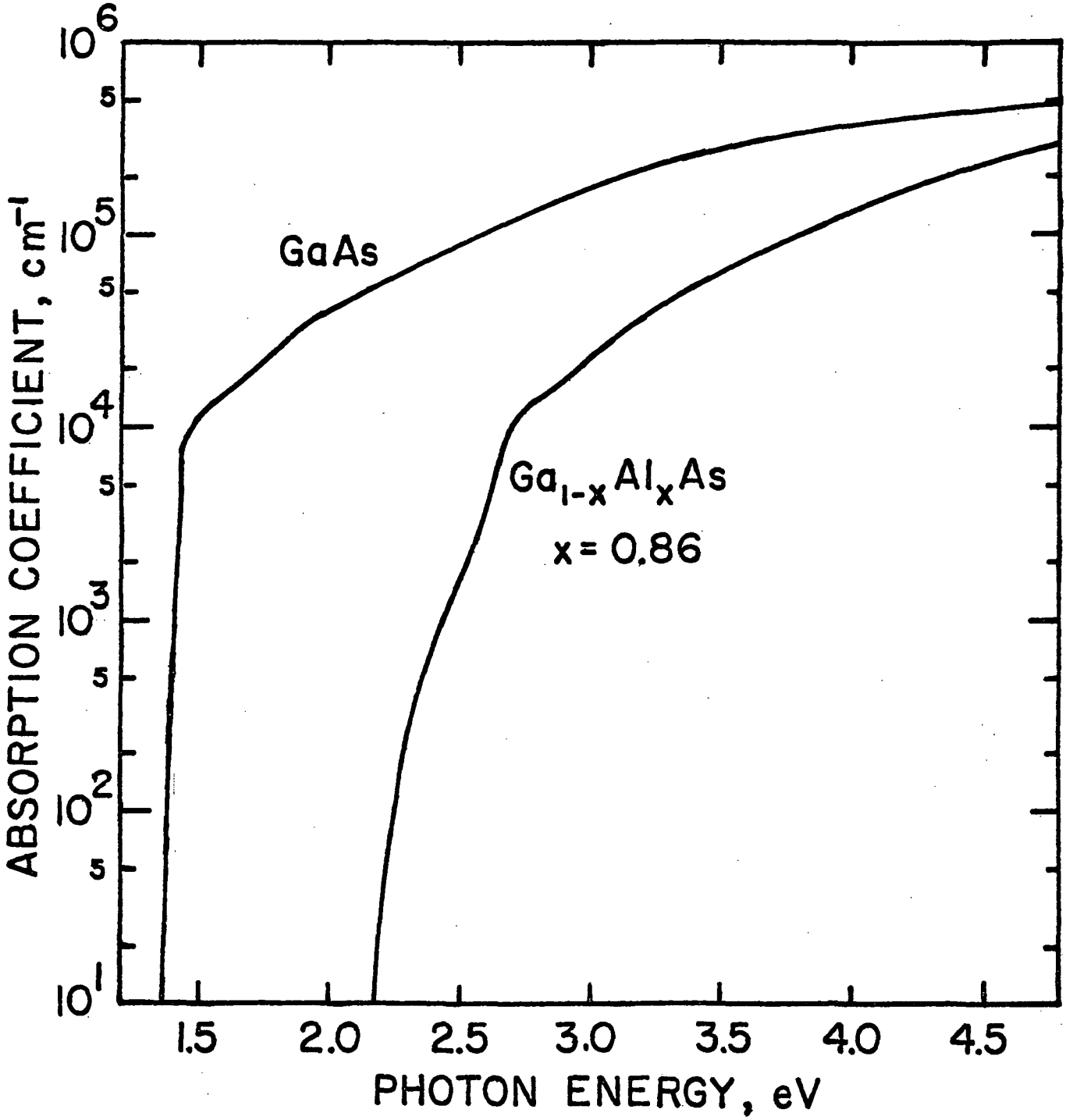
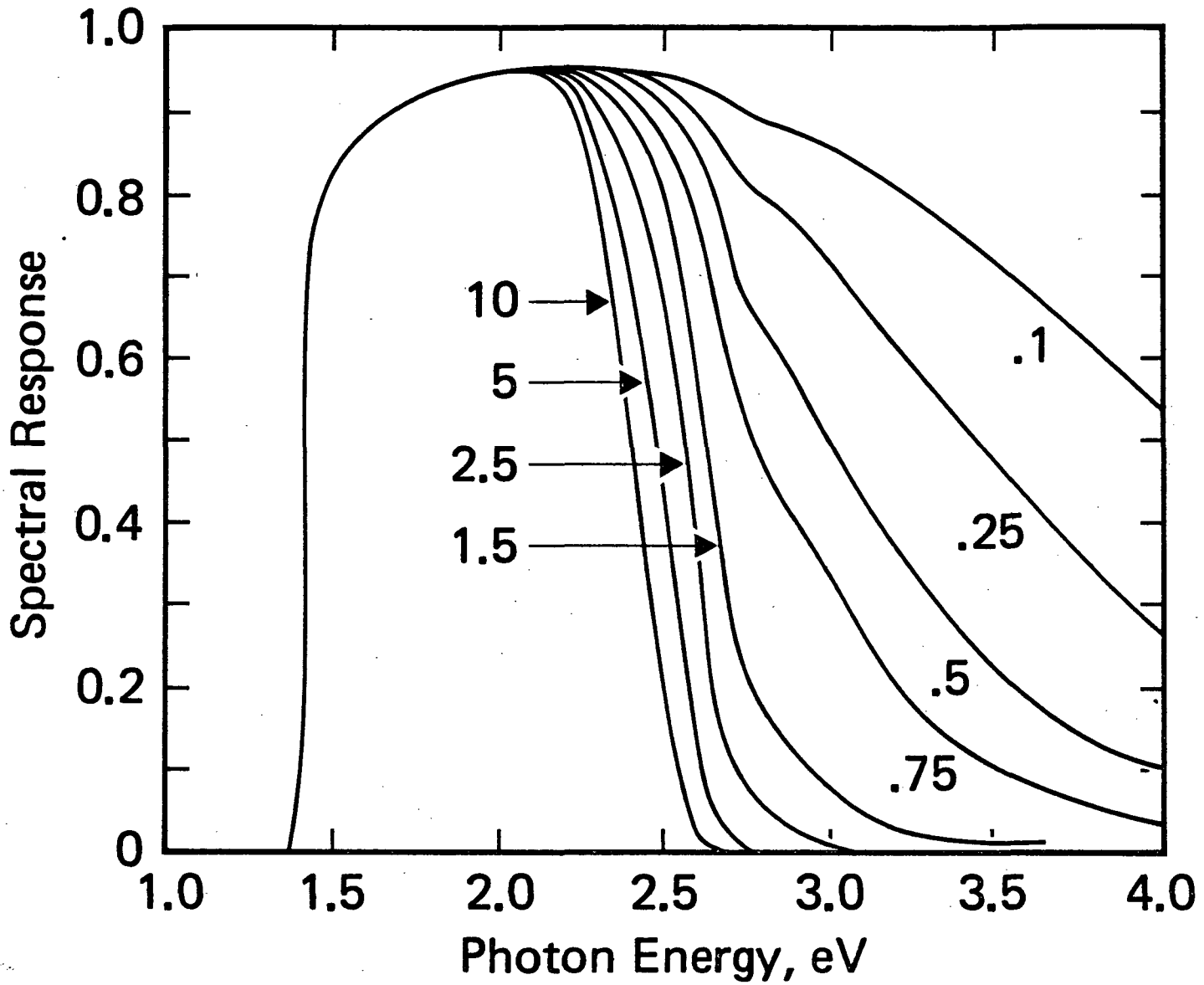


Figure 6



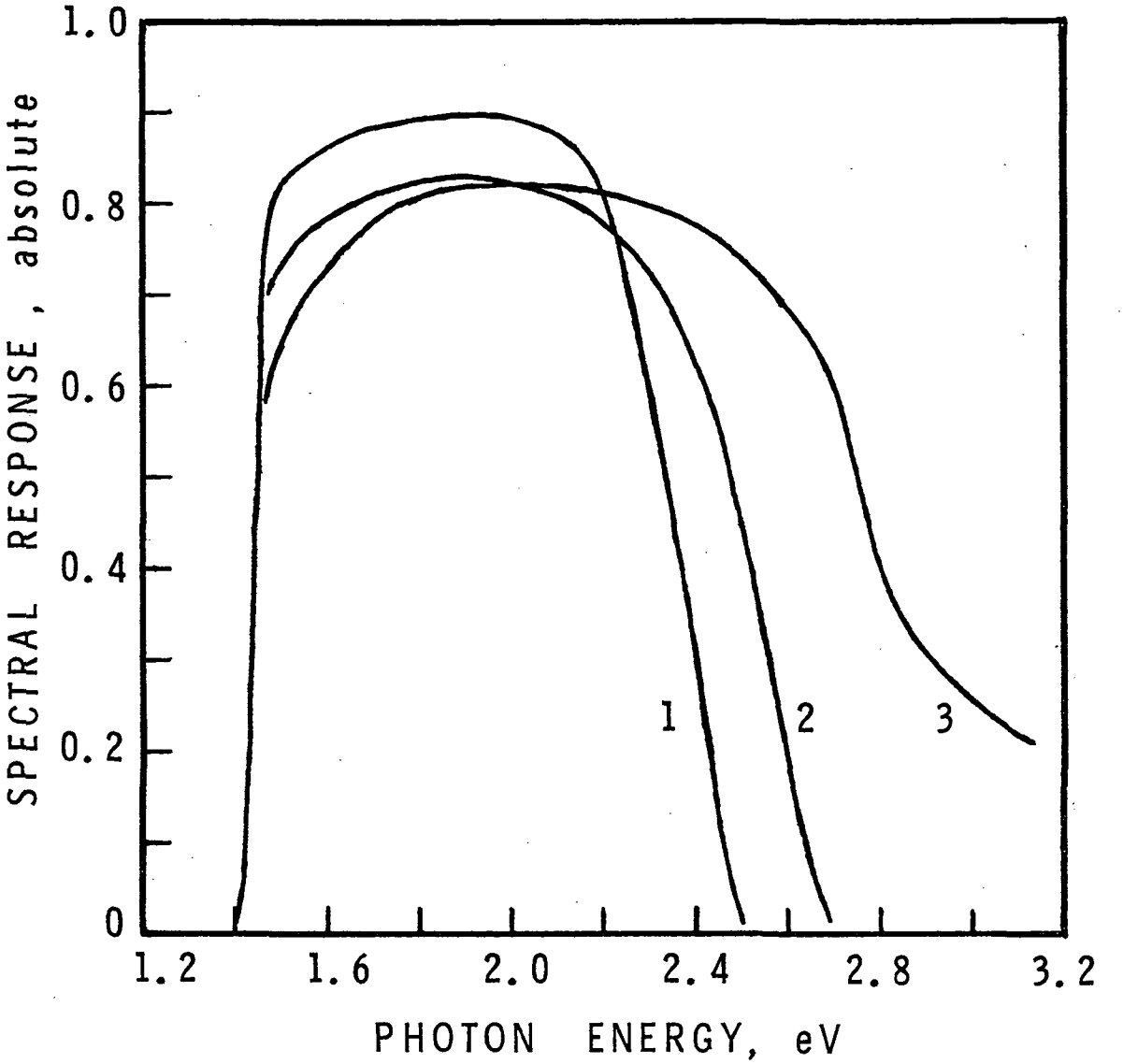
Absorption coefficients.

Figure 7



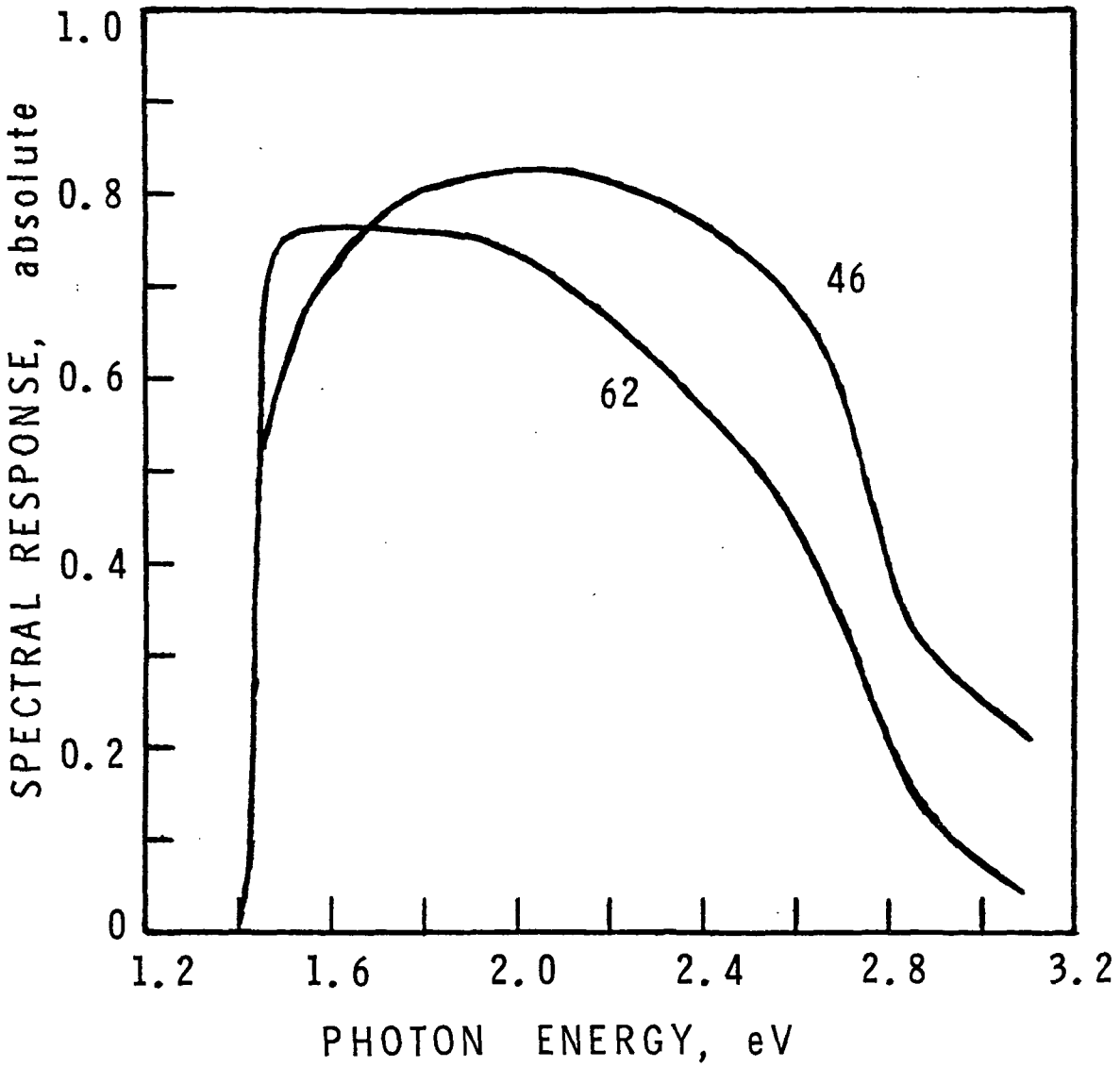
Spectral responses for decreasing GaAlAs thickness, parameters of Table 1.

Figure 8



Measured spectral responses. 1: x_j=0.8u, D=5.5u ; 2: x_j=1.1u, D=1.8u ; 3: x_j=1.1u, D=0.6u.

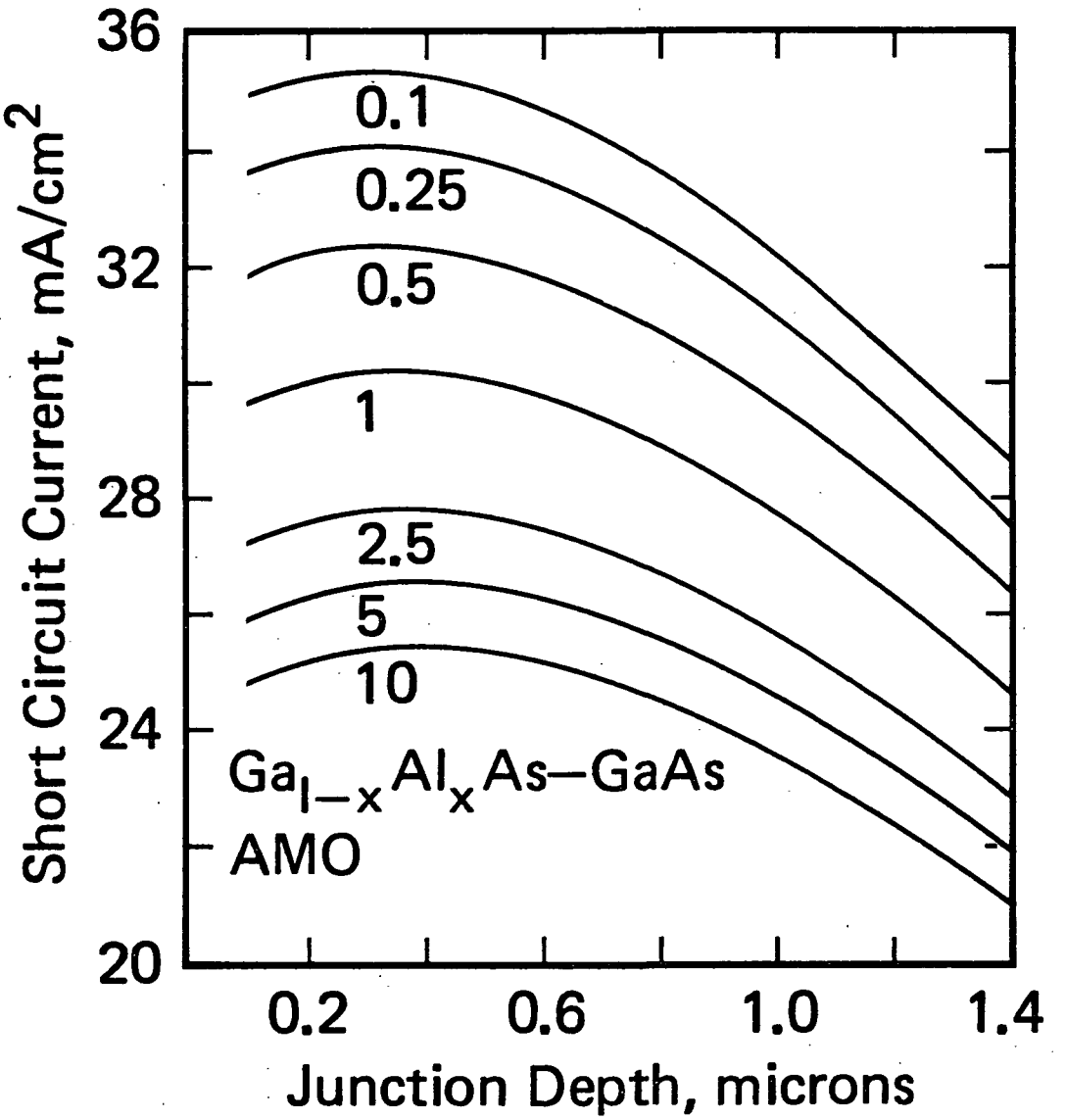
Figure 9



Measured spectral responses, GaAlAs = 0.6u.

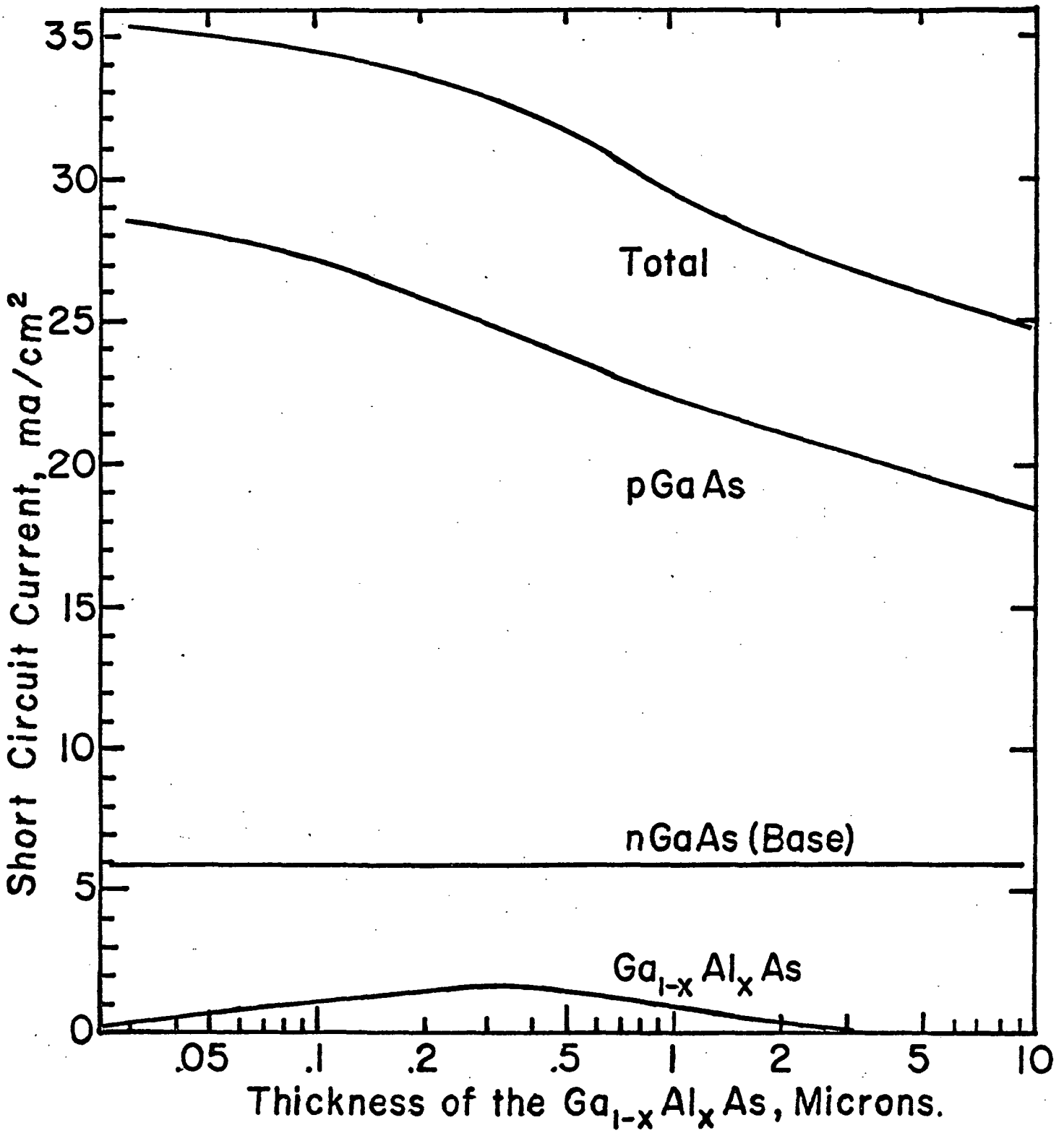
scb46, x_j = 1.1 μ; scb62, x_j = 3.0 μ.

Figure 10



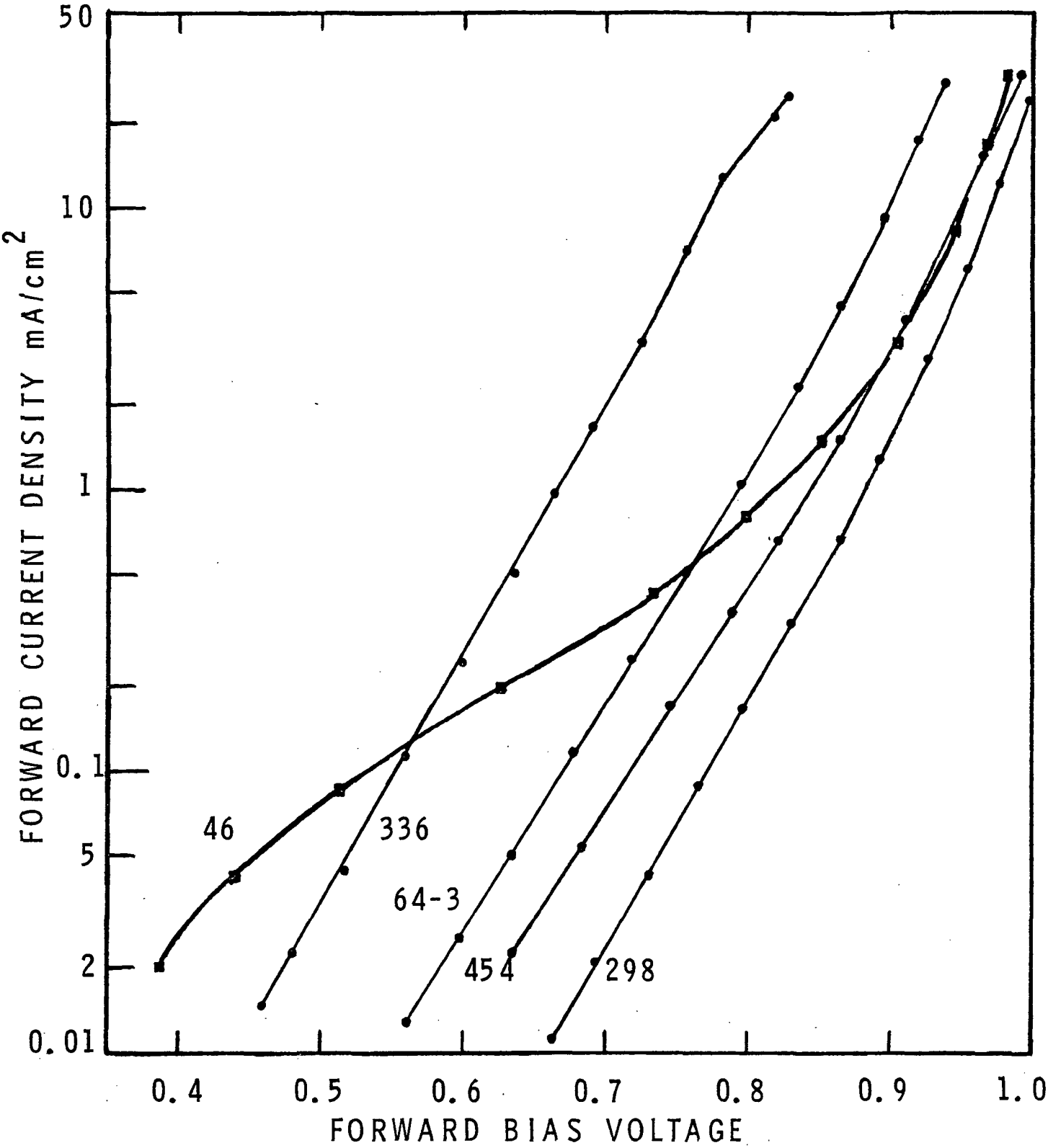
Short circuit current versus GaAlAs thickness. Parameters of Table 1.

Figure 11



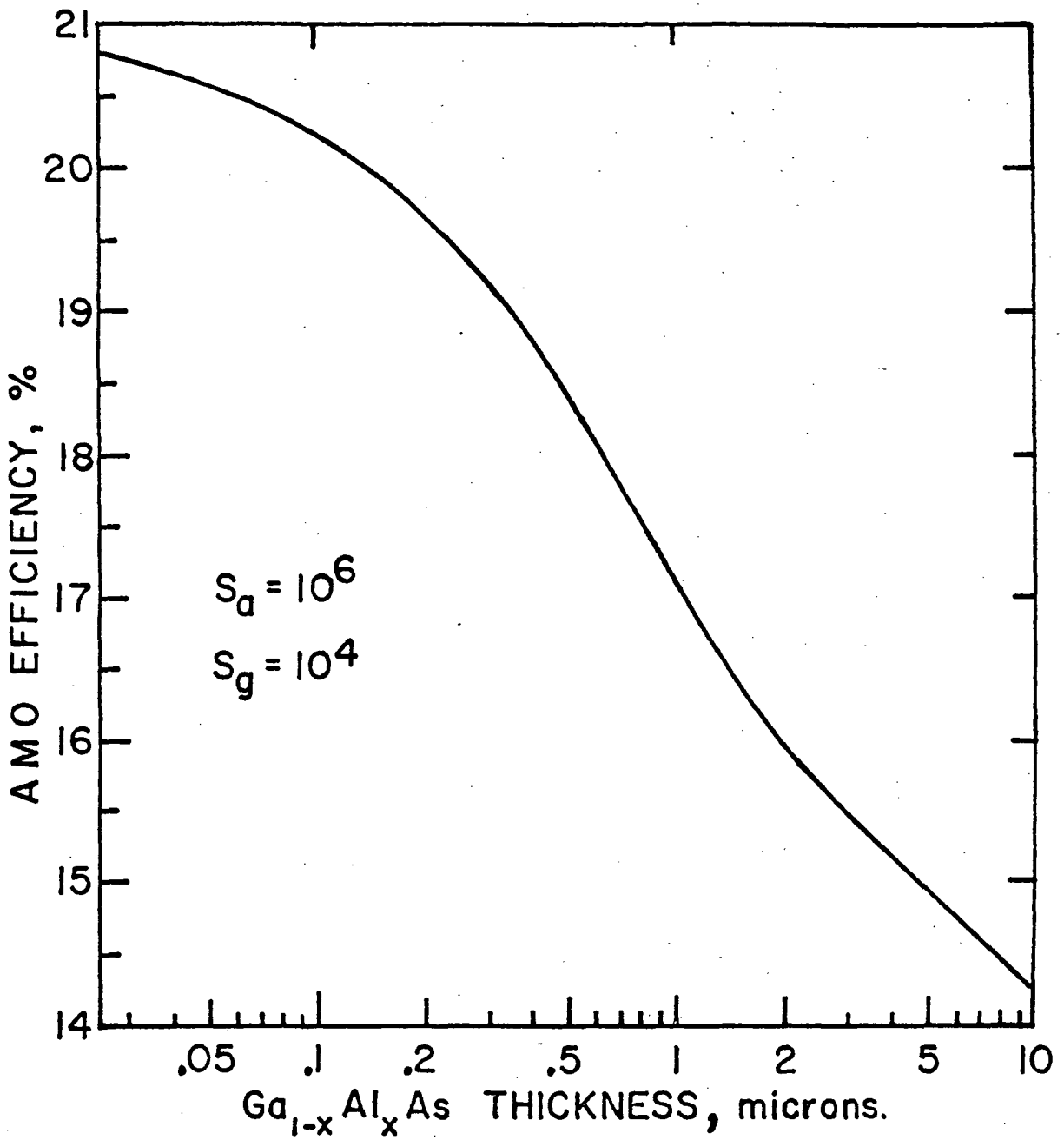
Short circuit current contributions. Parameters of Table 1. x_j = 0.5u.

Figure 12



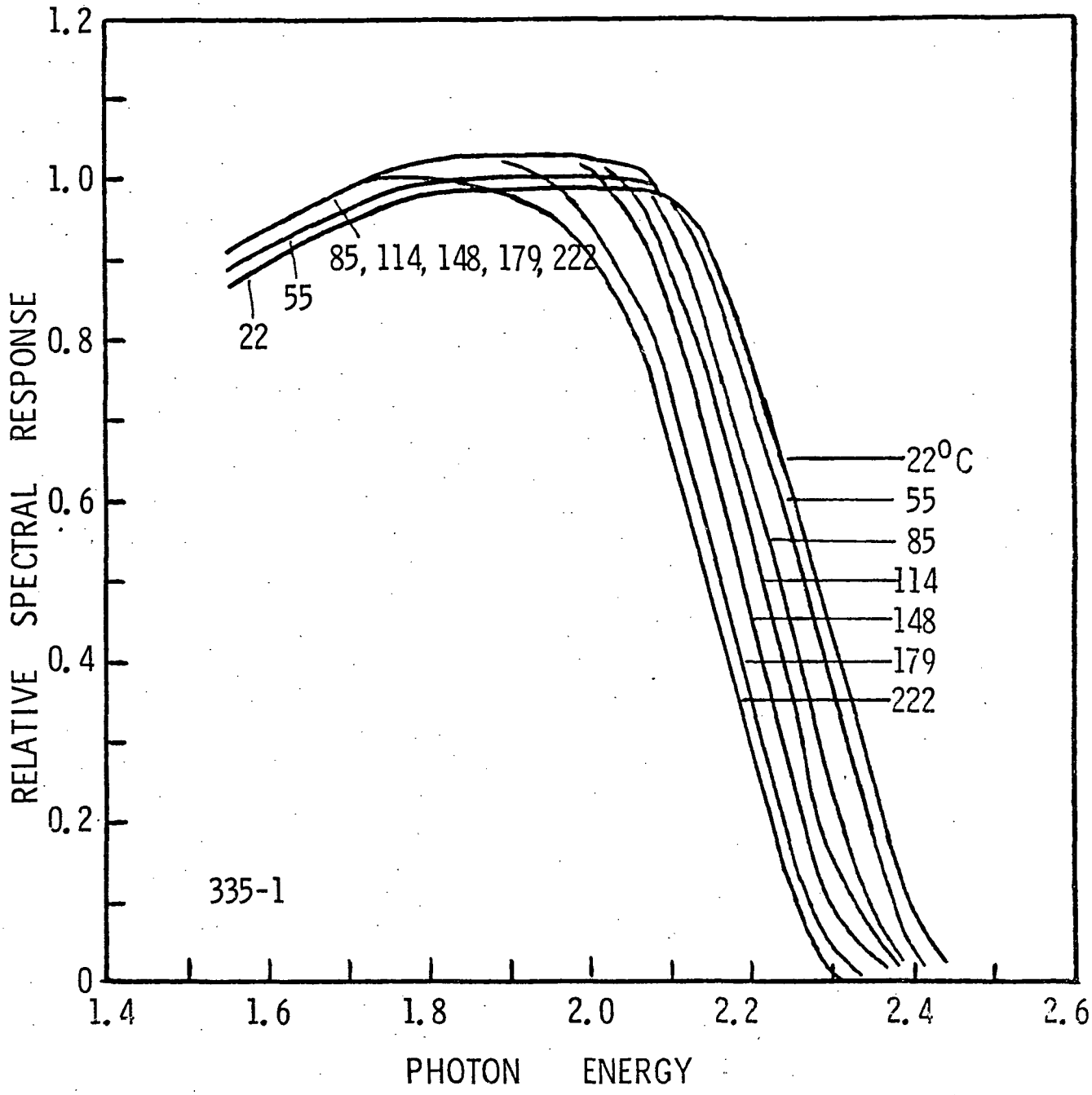
Measured current-voltage characteristics.

Figure 13



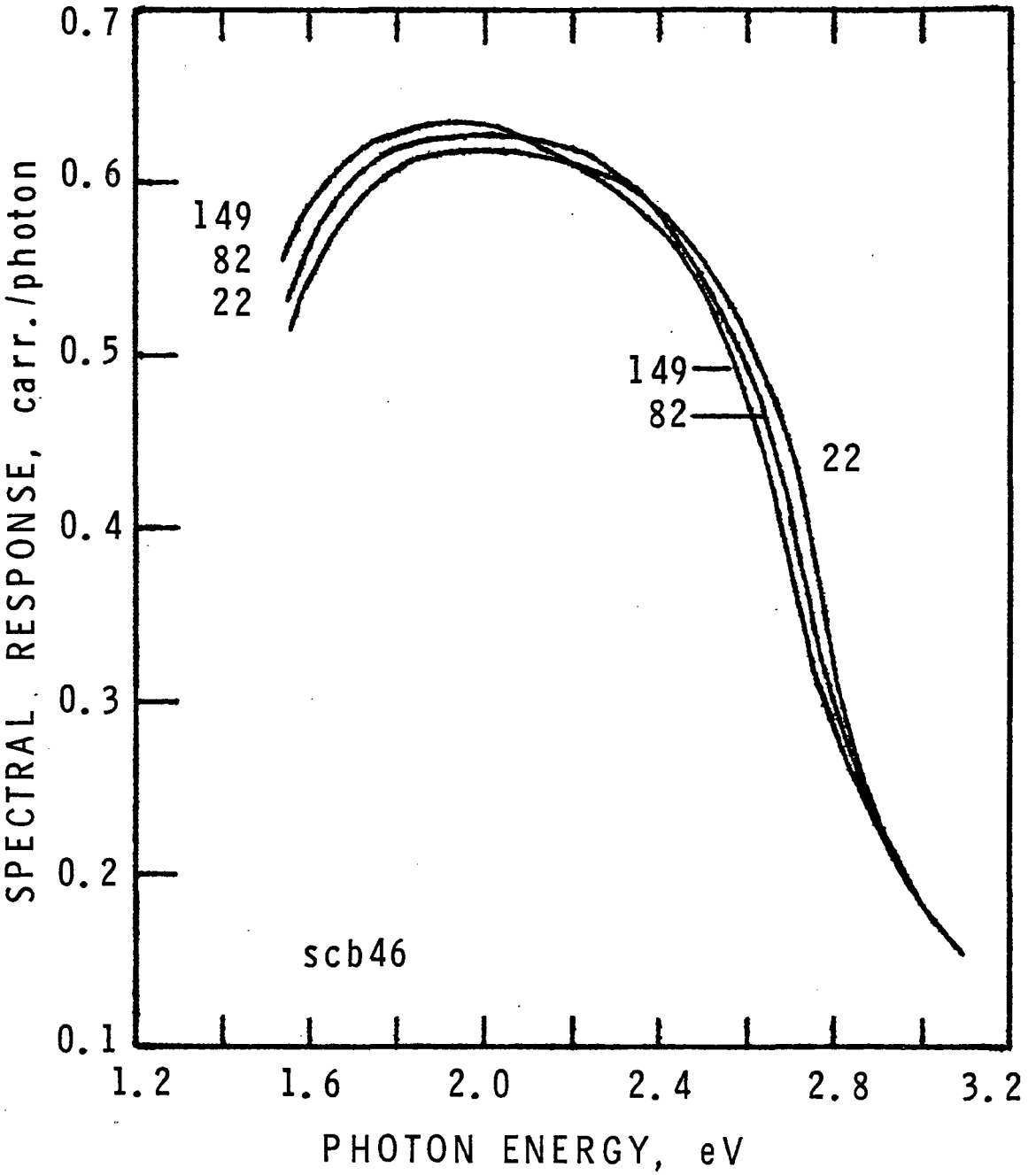
Calculated AMO efficiencies versus GaAlAs thickness. Parameters of Table 1, x_j = 0.5u.

Figure 14



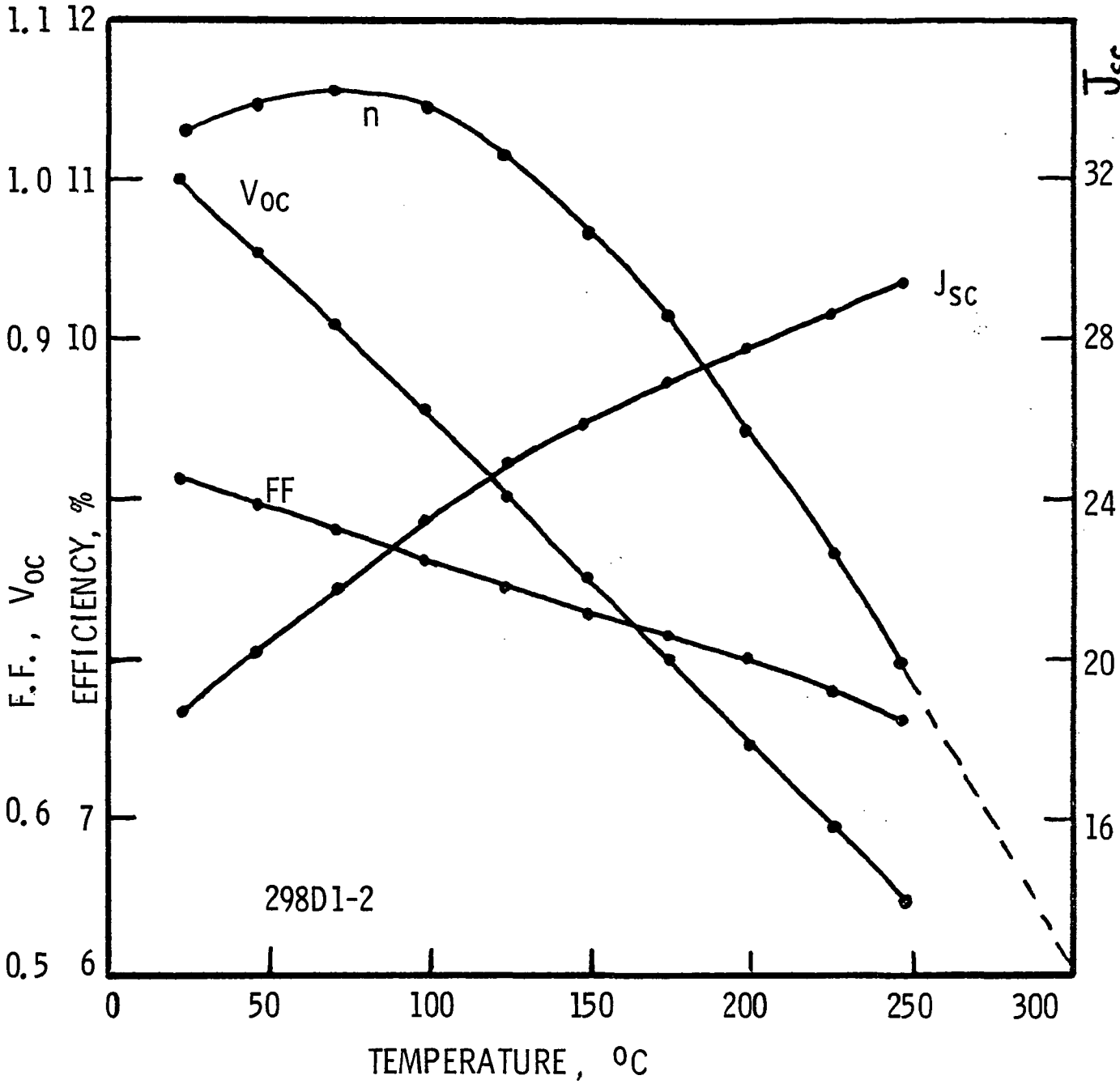
VARIATION OF $Ga_{1-x}Al_xAs$ BANDGAP WITH TEMP.

Figure 15



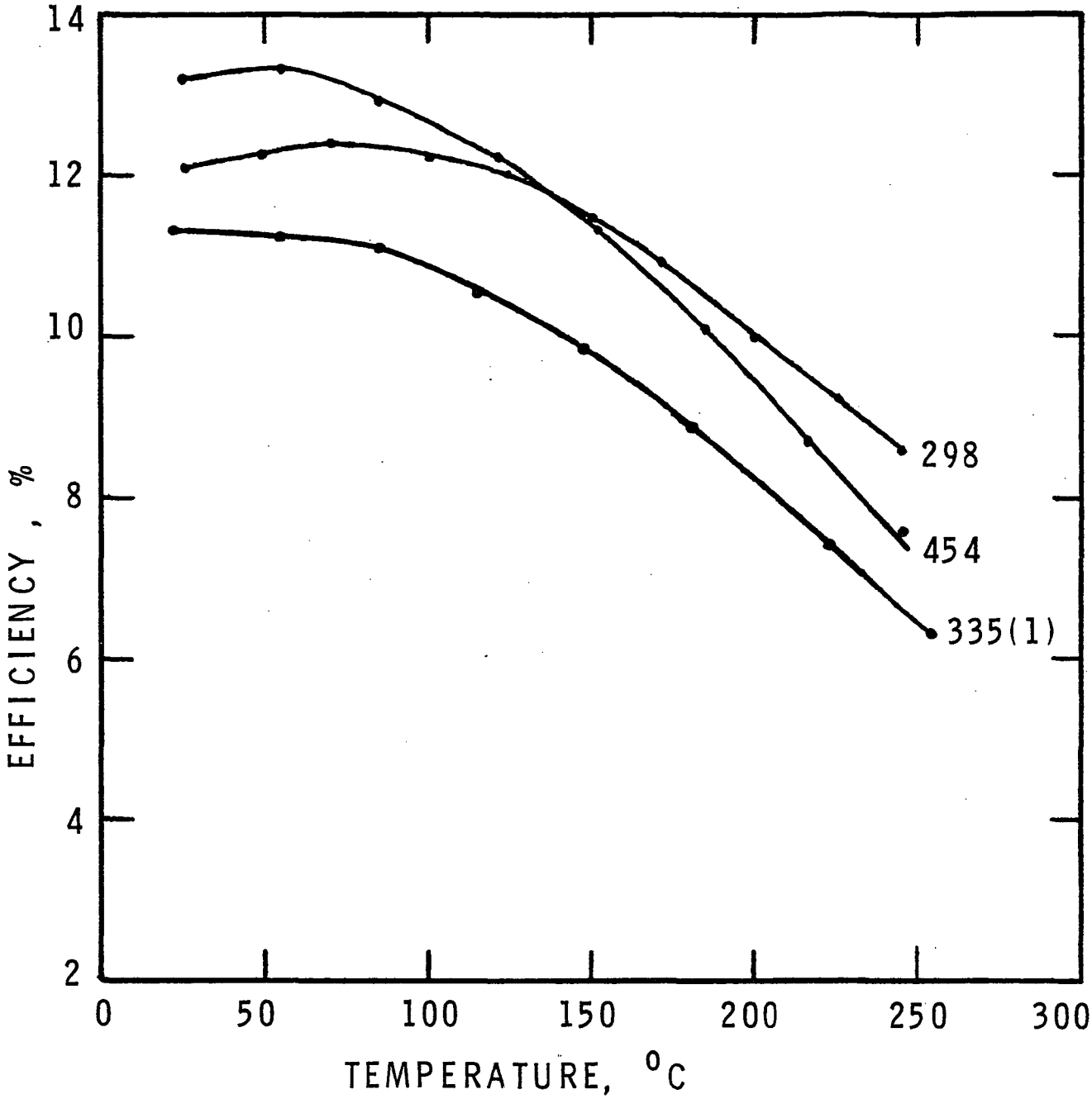
Spectral responses of a device with thin GaAlAs layer, D = 0.6u.

Figure 16



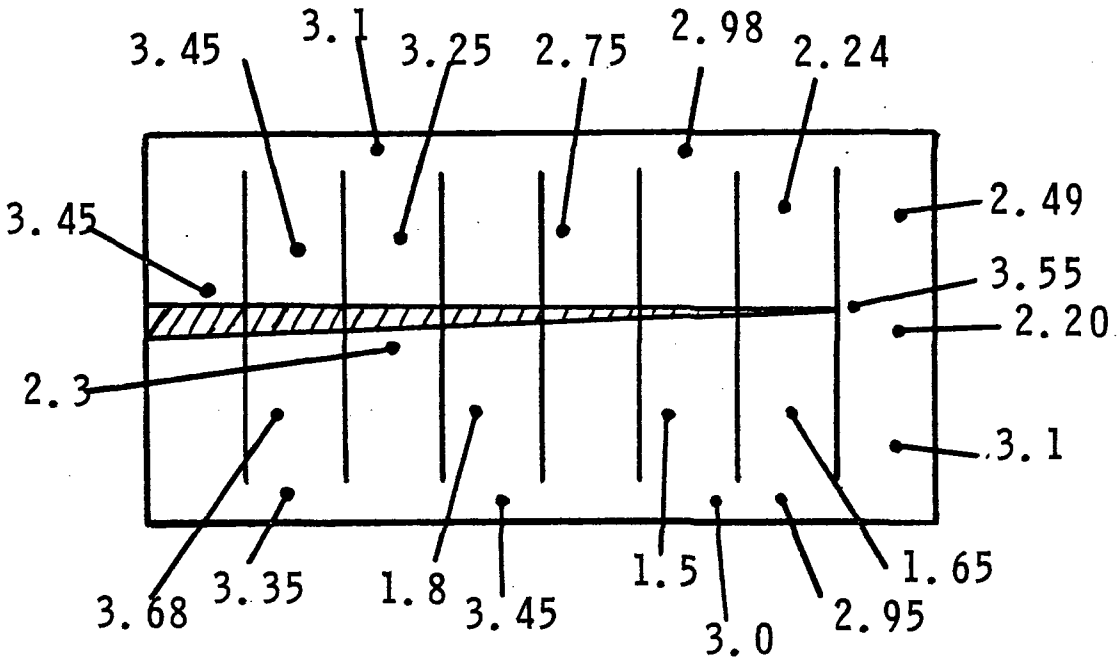
DEVICE PARAMETERS AS A FUNCTION OF TEMPERATURE

Figure 17



Measured efficiencies (contact area corrected).

Figure 18



Quantum efficiency variations at 6328A. The numbers are in 10^{-1} milliamps.

Figure 19